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LOGICAL METHOD OF CONTROL OF OPERATION
OF ELECTRIC NETWORKS

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LOGICAL METHOD OF CONTROL OF OPERATION
OF ELECTRIC NETWORKS

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I. A. Chegis and S. V. Yablonskiy

LOGICAL METHOD OF CONTROL OF OPERATION OF
ELECTRIC NETWORKS

Introduction

In the operation of complicated networks, even when they are made up of reliable elements, the probability of appearance of faults becomes considerable. Therefore, in the operation of complicated networks, particular attention attaches to the problem of monitoring the operation of these devices, ^{and} of methods of finding faults. However, by virtue of the complexity of networks, the process of finding faults requires a great loss of time and high skill on the part of the service personnel. These circumstances have led the authors to engage in the development of a mathematical formalism, which permits, at a relatively small number of tests (ringing), to determine the place and the character of the fault. The basic results in this direction were obtained in 1954 and were reported at the session of the Moscow Mathematical Society in 1955 [5]. The constructed rules make it possible to automatize the process of control of the operation of the device. In the case of manual control, they also are of considerable effectiveness, since because

of their algorithmic nature they can be performed by workers of low skill and within a short time.

In the present article we expound in detail this problem. The general theory developed in this paper is based on the following premises.

1) A network \mathcal{N} is specified, and when it is in working order it realizes a certain function $f(x_1, x_2, \dots, x_n)$, specified on the set E .

2) There is a list of possible faults (which are not of random character) with an indication of the number of simultaneously possible faults; with this, to each possible combination of faults there corresponds a function defined on the set E .

3) Methods of carrying out the control are described.

Consequently, the results of this general theory are applicable only to networks for which a logical description has been developed. Therefore, for illustration, we have used contact networks. This choice was dictated also by the fact that contact networks represent, from the point of view of reliable means, the most simple networks, hence the necessary step towards studying the more complicated networks.

In addition, a whole series of questions was considered exclusively for contact networks.

As applied to contact networks, premises 1, 2, and 3 are formulated as follows.

- 1) Corresponding to contact network \mathcal{O} is a function $f(x_1, x_2, \dots, x_n)$ of algebraic logic.
- 2) Two kinds of faults are considered -- the short circuiting of the contact and the opening of the contact; so far no limitations are imposed on the number of simultaneously possible faults.
- 3) The network is monitored on the basis of its response to different various combinations of the states of the relays.

Example. The network shown in Fig. 1 realizes the function $f(x_1, x_2) = x_1 + x_2 + 1 \pmod{2}$. Let it be required to find a fault in the network, if it is known that one contact is faulty. It is easy to see that for this purpose it is enough to establish whether or not the network conducts under the following states of the relays

$$x_1 = 0, x_2 = 0; x_1 = 0, x_2 = 1; x_1 = 1, x_2 = 0; x_1 = 1, x_2 = 1.$$

Namely: if when $x_1 = x_2 = 0$ the circuit does not conduct, then either contact 2 is open or contact 4 is open; if when $x_1 = x_2 = 1$ the circuit does not conduct, then either contact 1 is open or contact 3 is open; if when $x_1 = 0$ and $x_2 = 1$ the circuit does conduct, then either

contact 1 or contact 4 is closed; if when $x_1 = 1$ and $x_2 = 0$ and the circuit conducts, then either 2 or contact 3 is closed.

The article consists of two chapters. In Chap. I are considered general problems of control of networks, that is to say, without taking into account the structure of the network. A general procedure is given for the construction of tests. For illustration we give several examples from the field of contact networks. The measures developed for the construction of minimal tests can be used directly for the construction of minimal disjunctive (or conjunctive) normal forms [6]. At the end of the chapter we establish a duality principle for tests and disclose certain properties of single tests as applied to contact networks. What remains unstudied are the possibilities of control by means of conscious modification of the topology of the network; for example, short circuiting between any two vertices of the network, the removal of part of the network, the rearrangement of the blocks, etc. In Chap. II procedure is given for the construction of tests for individual classes of networks with account taken of the structure of the networks. The latter is due to the fact that the general algorithm, even for relatively simple contact networks (which realize functions of 6 or 8 variables)

becomes too cumbersome. Therefore, as in the case of network synthesis, it was logical to narrow down the class of networks and thereby increase the effectiveness. The procedure of construction the tests is based here on a block construction of the network and on an inductive specification of the functions. In this manner the construction of tests reduces to the construction of tests for individual blocks. In the latter case the consideration of the general theory are used. Next to be studied are tentative and ordered texts.

The results of Chap. I and Chap. II, Sec. 7 were derived by S. V. Yablonskiy; the remaining results were obtained by I. A. Chegis. The general writing of the text was performed by S. V. Yablonskiy. The work on the formulation and calculation of the examples was carried out by T. A. Alferova and L. N. Rybakova, to whom the authors express their gratitude.

Chapter I

General Theory of Construction of Tests

1. Tables of Fault Functions and Methods of Their Construction

Let a network Ω consist of l elements (for example, contacts). Let furthermore the element i have s_i faults. It is obvious that the number of different

faults in the network is equal to

$$\prod_{i=1}^k (1 + s_i) - 1.$$

Let us renumber the faults of interest to us. Then, for the j -th fault the network \mathcal{O}_i goes into the network \mathcal{O}_j . We denote by $f_j(x_1, x_2, \dots, x_n)$ the function corresponding to the work of the network \mathcal{O}_j . The function $f_j(x_1, x_2, \dots, x_n)$ is called the fault function.

Let M be the set of investigated faults. Then a table of functions, containing a table of functions $f(x_1, x_2, \dots, x_n)$ *, and also the tables of all the fault functions $f_a(x_1, x_2, \dots, x_n)$, where $a \in M$, is called the table of fault functions.

* We make the correct state of the network correspond to the index 0, and then, by definition, the function $f_0(x_1, x_2, \dots, x_n) \equiv f(x_1, x_2, \dots, x_n)$.

There exist two methods of constructing tables of fault functions.

The first method consists of constructing the table by rows. For this purpose one scans all the assemblies of the values of the arguments. For each value of the argument one seeks the corresponding value of the function f , and one marks on the

diagram the contacts, either with a solid line or with a dotted line, depending on whether the contact closes or opens at the particular assembly. Then, for $f = 0$, one picks out those faults which short the network, and in the according columns of the row under consideration one places a "1". At $f = 1$, one picks out those faults, which open the circuit, and on the corresponding columns of the row under consideration one places a "0". Then after scanning all the assemblies one obtains a table of fault functions. In each column of the table, corresponding to a given fault, one obtains a table of the functions of this fault, and into the empty boxes one should transfer mentally the corresponding values of the function f_0 .

Example. Let us consider the sequence of compiling a table of fault functions in accordance with the indicated first method, for the network shown in Fig. 2, which realizes the function $S_{1,3,4}(x, y, z, w)$, and the assumed faults are the closing or opening of a single contact. For convenience, we number the contacts of the network (see Fig. 2) from 1 to 14. ^{The} Distribution of the faults is shown in Table 1.

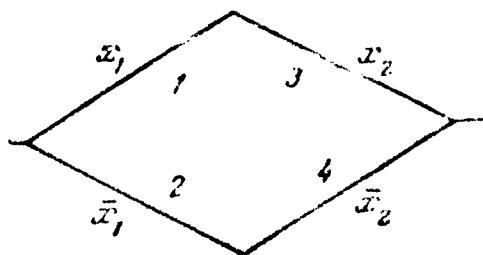


Fig. 1

Table 1

(x, y, z, u)	0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	1'	2'	3'	4'	5'	6'	7'	8'	9'	10'	11'	12'	13'	14'
(0, 0, 0, 0)	0	1			1		1		1		1		1		1														
(0, 0, 1, 1)	0	1			1			1		1		1		1		1													
(0, 1, 0, 1)	0	1			1		1	1	1		1		1		1														
(0, 1, 1, 0)	0	1			1		1	1	1		1		1		1														
(1, 0, 0, 1)	0		1	1		1		1		1		1		1		1													
(1, 0, 1, 0)	0		1	1		1		1		1		1		1		1													
(1, 1, 0, 0)	0		1	1		1										1	1												
(0, 0, 0, 1)	1															0	0	0	0	0	0	0	0	0	0	0	0	0	0
(0, 0, 1, 0)	1															0	0	0	0	0	0	0	0	0	0	0	0	0	0
(0, 1, 0, 0)	1															0	0	0	0	0	0	0	0	0	0	0	0	0	0
(0, 1, 1, 1)	1															0	0	0	0	0	0	0	0	0	0	0	0	0	0
(1, 0, 0, 0)	1															0	0	0	0	0	0	0	0	0	0	0	0	0	0
(1, 0, 1, 1)	1															0	0	0	0	0	0	0	0	0	0	0	0	0	0
(1, 1, 0, 1)	1															0	0	0	0	0	0	0	0	0	0	0	0	0	0
(1, 1, 1, 0)	1															0	0	0	0	0	0	0	0	0	0	0	0	0	0
(1, 1, 1, 1)	1															0	0	0	0	0	0	0	0	0	0	0	0	0	0

$$f_7 = f_9,$$

$$f_r = f_{10},$$

$$f_{13} = f_{15},$$

In this table, the first column (x, y, z, w) contains all possible assemblies, whereas the succeeding columns are headed with the numbers 0, 1, 2, ..., 14 and $1', 2', \dots, 14'$, where the number 0 corresponds to the correct state of this network, and each of the numbers 1, 2, ..., 14 corresponds to the closing of the contact denoted by the same number on Fig. 2, and to each of the numbers $1', 2', \dots, 14'$ corresponds an opening of the same contact.

Figs. 3 and 4 show sketches of each assembly indicated in Table 1; the asterisks mark the contacts, the closing (Fig. 3) or opening (Fig. 4) each of which brings the circuit to a closed or to an open state. Over each network is written out the corresponding assembly, and under each network the numbers of these faults are individually written.

To explain the manner with which the construction of Table 1 is carried out and with which the indicated diagrams of Figs. 3 and 4 are drawn, let us consider the assembly $(0, 0, 0, 0), S_{1,3,4}(0, 0, 0, 0) = 0$. Corresponding to it is the correct state of the system indicated in the upper left corner of Fig. 3. Comparing this circuit with the row of Table 1 corresponding to the assembly $(0, 0, 0, 0)$ and with

L

Fig. 2, we see that in the table one places a "1" in the columns with numbers corresponding to the numbers of the contacts marked with asterisks (i.e., in columns 1, 5, 7, 9, and 12).

In the second method the table is constructed by columns. For this purpose one introduces a fault in the network, i.e., certain contacts are short circuited and others are discarded. After such an operation, a network with the particular fault under consideration is obtained. This network corresponds to the fault function of interest to us. However, sometimes there is no need for compiling again a function of this fault. In fact, assume that a certain contact has opened. Let us consider all the circuits which pass through this contact. We write out all the assemblies corresponding to these circuits. Obviously, the fault function (corresponding to the opening of the contact under consideration) can differ from the original function $f(x_1, x_2, \dots, x_n)$ only at the written out assemblies, or more accurately, the difference takes place, if the written assemblies are not encountered in any circuit that does not pass through the given contact, and to the contrary, the difference in a certain assembly does not take place if this assembly is encountered at least in one such circuit.

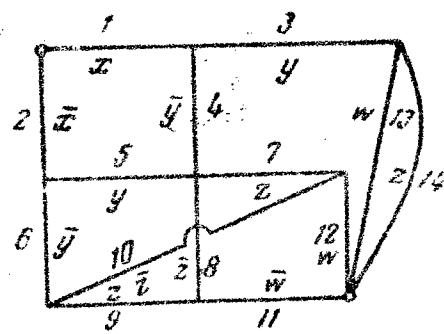


Fig. 2

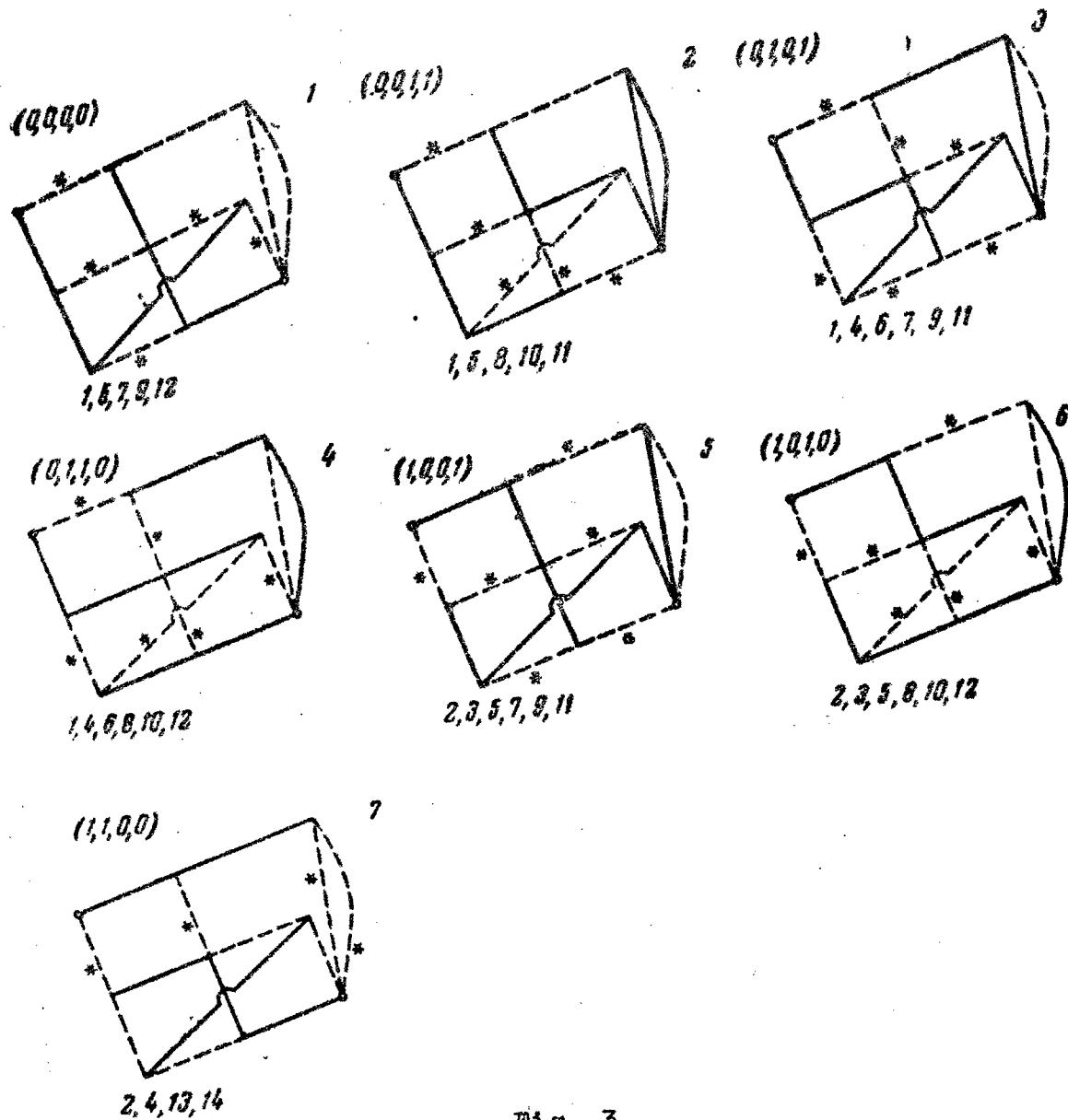


Fig. 3

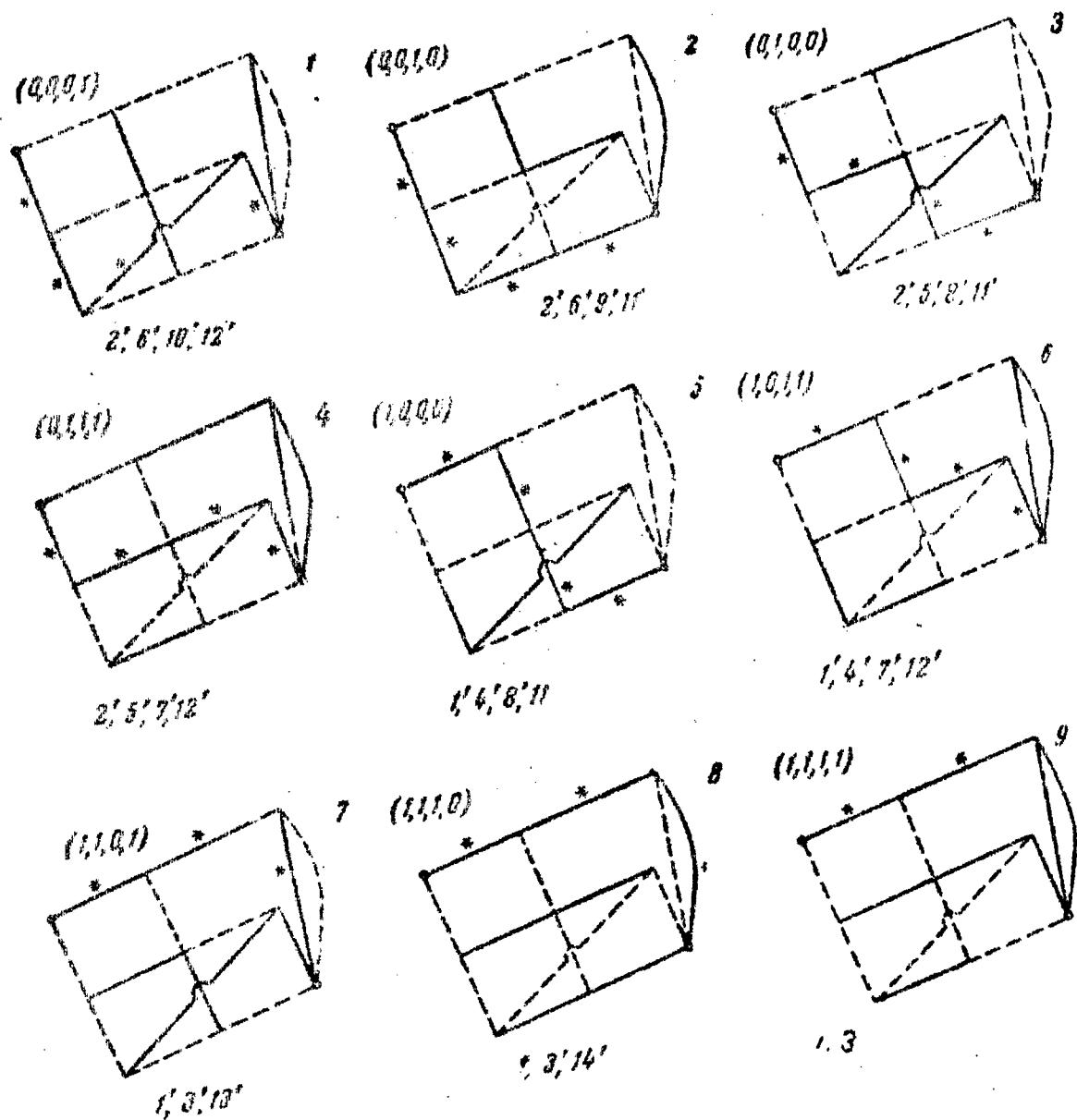


Fig. 4

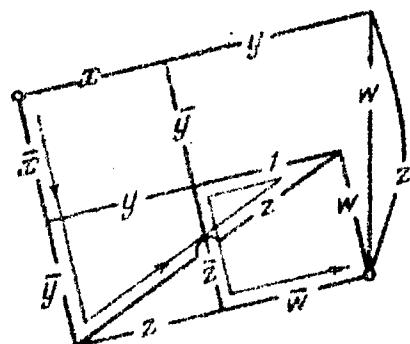


Fig. 5

Assume that the fault consists of a shorted contact.⁷ Let us consider all the circuits which have passed through this contact, eliminating those in which a contact identical with that considered is involved. Again we write out all the assemblies corresponding to these circuits. In the assemblies we change the values corresponding to the given contact to the opposite ones. The fault function either does not differ from the original function at the constructed assemblies, or differs from it, depending on whether or not these assemblies are encountered in the circuits that do not pass through the given contact. However, the difference in the fault function from $f(x_1, x_2, \dots, x_n)$ can take place also at other assemblies, which correspond to the so called "false circuit," i.e., circuits different from those considered above. An example of a network with a false circuit is shown in Fig. 5.

Example. Let us consider the order of compiling a table of fault functions in accordance with the second method for the preceding circuit (see Fig. 2).

Shorts. Fig. 6 shows the circuits that are produced from the initial one (see Fig. 2) from closing of any given single contact. On the diagrams of Fig. 6 these contacts are denoted by the number 1, which

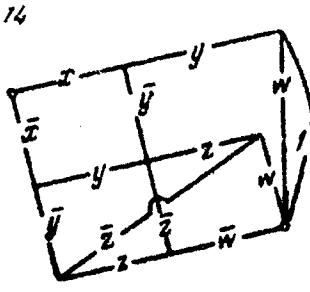
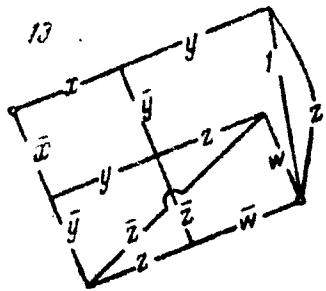
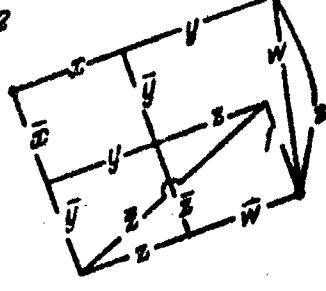
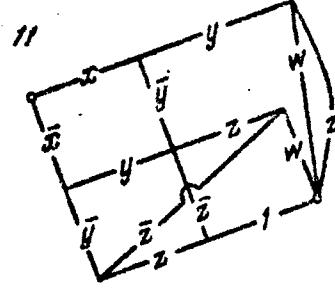
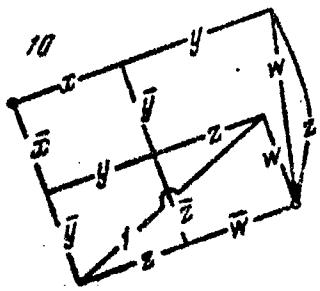
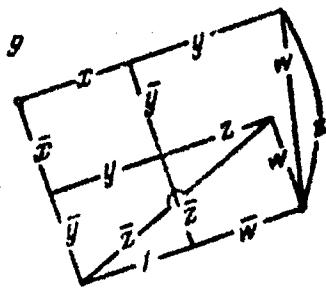
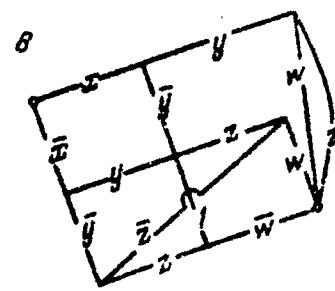
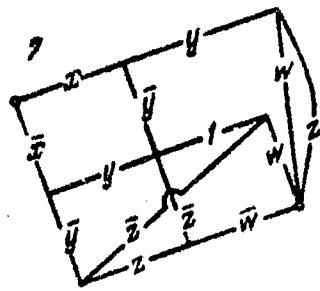
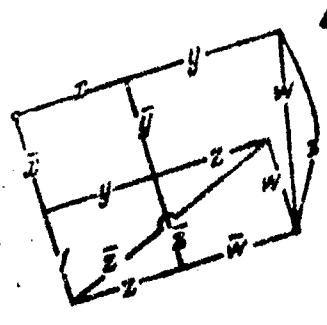
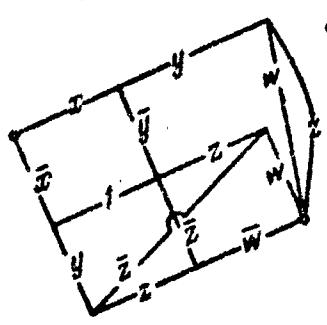
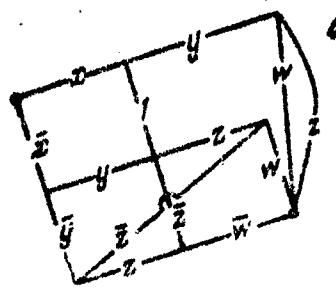
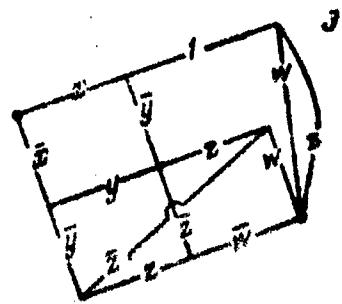
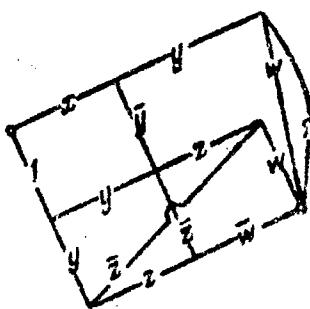
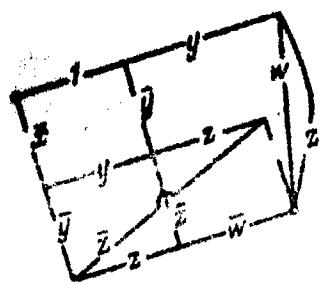


Fig. 6

designates an identical admittance.

Analyzing Fig. 6, we obtain functions that describe the corresponding admittances of the networks (i.e., the fault functions for a given network):

$$f_1 = S_{1,3,4}(x, y, z, w) \vee xyz \vee xyw \vee x\bar{y}zw \vee x\bar{y}z\bar{w},$$

$$f_2 = S_{1,3,4}(x, y, z, w) \vee x\bar{y}z\bar{w} \vee x\bar{y}zw \vee x\bar{y}z\bar{w},$$

$$f_3 = S_{1,3,4}(x, y, z, w) \vee x\bar{y}z \vee x\bar{y}w,$$

$$f_4 = S_{1,3,4}(x, y, z, w) \vee x\bar{y}z\bar{w} \vee x\bar{y}z \vee x\bar{y}w,$$

$$f_5 = S_{1,3,4}(x, y, z, w) \vee x\bar{y}z\bar{w} \vee x\bar{y}zw \vee x\bar{y}z\bar{w} \vee x\bar{y}z\bar{w},$$

$$f_6 = S_{1,3,4}(x, y, z, w) \vee x\bar{y}z\bar{w} \vee x\bar{y}z\bar{w},$$

$$f_7 = S_{1,3,4}(x, y, z, w) \vee x\bar{y}z\bar{w} \vee x\bar{y}zw \vee x\bar{y}z\bar{w},$$

$$f_8 = S_{1,3,4}(x, y, z, w) \vee x\bar{y}z\bar{w} \vee x\bar{y}zw \vee x\bar{y}zw,$$

$$f_9 = S_{1,3,4}(x, y, z, w) \vee x\bar{y}z\bar{w} \vee x\bar{y}zw \vee x\bar{y}zw,$$

$$f_{10} = S_{1,3,4}(x, y, z, w) \vee x\bar{y}z\bar{w} \vee x\bar{y}zw \vee x\bar{y}zw,$$

$$f_{11} = S_{1,3,4}(x, y, z, w) \vee x\bar{y}z\bar{w} \vee x\bar{y}zw \vee x\bar{y}zw,$$

$$f_{12} = S_{1,3,4}(x, y, z, w) \vee x\bar{y}z\bar{w} \vee x\bar{y}zw \vee x\bar{y}z\bar{w},$$

$$f_{13} = S_{1,3,4}(x, y, z, w) \vee xy\bar{w},$$

$$f_{14} = S_{1,3,4}(x, y, z, w) \vee xyz.$$

Here the numbers of the function f correspond to the numbers of the networks on Fig. 6.

Open circuits: Analogously, on Fig. 7 we show the networks that are derived from the initial one upon opening of any single contact, and the contact

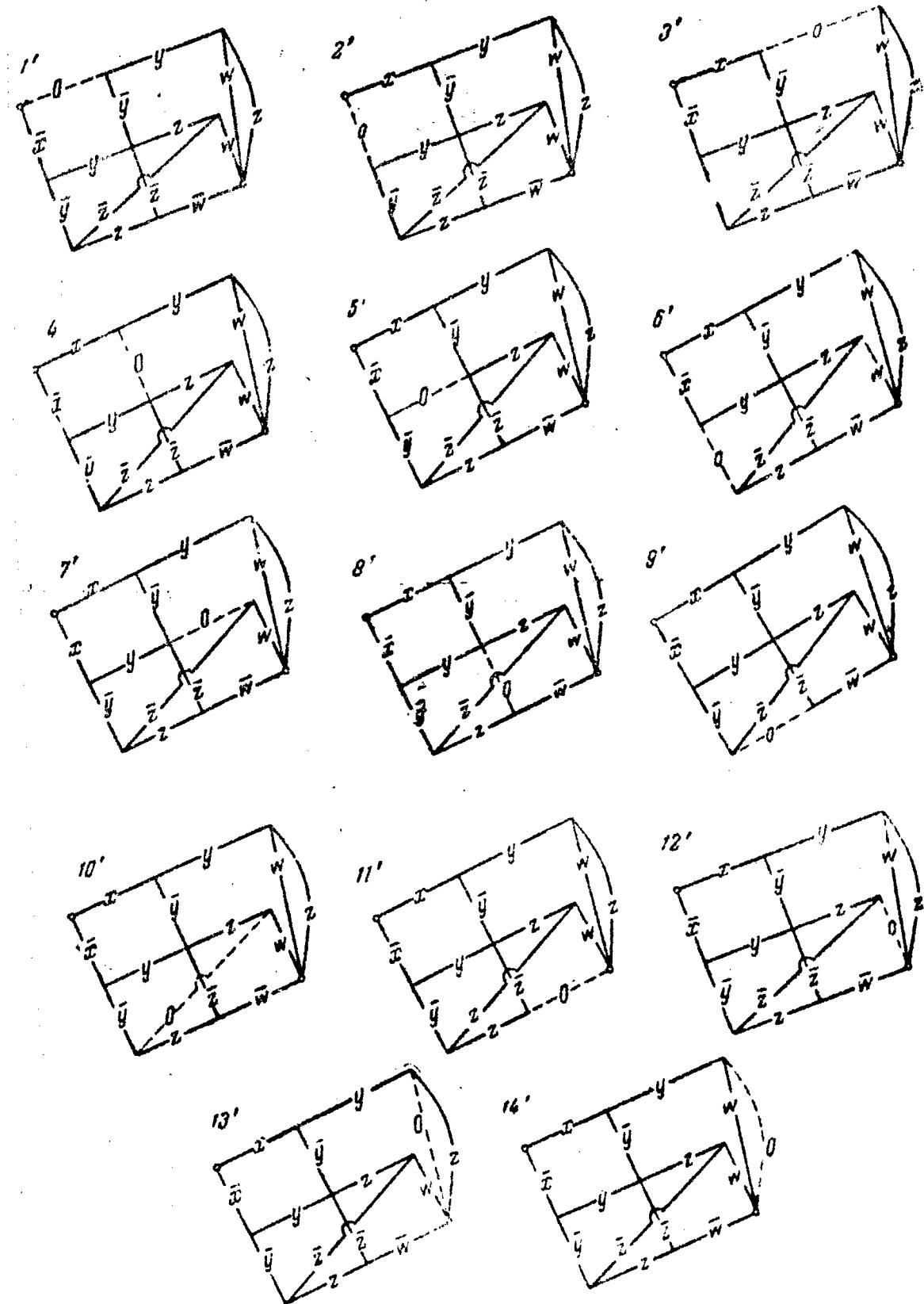


Fig. 7

in which the discontinuity takes place is denoted by zeros on these diagrams.

For each network shown in Fig. 7, we write out a function that describes the admittance of this network (i.e., the fault function for the given network):

$$\begin{aligned}
 f_1 &= xyzw \vee xy\bar{z}w \vee x\bar{y}zw \vee x\bar{y}\bar{z}w, \\
 f_2 &= xyz \vee xyw \vee x\bar{y}zw \vee x\bar{y}\bar{z}w, \\
 f_3 &= xyzw \vee x\bar{y}zw \vee xyzw \vee xy\bar{z}w \vee x\bar{y}\bar{z}w \vee x\bar{y}\bar{z}\bar{w}, \\
 f_4 &= xyz \vee xyw \vee x\bar{y}zw \vee x\bar{y}\bar{z}w \vee x\bar{y}\bar{z}\bar{w}, \\
 f_5 &= xyz \vee xyw \vee x\bar{y}zw \vee x\bar{y}\bar{z}w \vee x\bar{y}\bar{z}\bar{w}, \\
 f_6 &= xyz \vee xyw \vee x\bar{y}zw \vee x\bar{y}\bar{z}w \vee x\bar{y}\bar{z}\bar{w}, \\
 f_7 &= xyz \vee xyw \vee x\bar{y}zw \vee x\bar{y}\bar{z}w \vee x\bar{y}\bar{z}\bar{w}, \\
 f_8 &= xyz \vee xyw \vee x\bar{y}zw \vee x\bar{y}\bar{z}w \vee x\bar{y}\bar{z}\bar{w}, \\
 f_9 &= xyz \vee xyw \vee x\bar{y}zw \vee x\bar{y}\bar{z}w \vee x\bar{y}\bar{z}\bar{w}, \\
 f_{10} &= xyz \vee xyw \vee x\bar{y}zw \vee x\bar{y}\bar{z}w \vee x\bar{y}\bar{z}\bar{w}, \\
 f_{11} &= xyz \vee xyw \vee x\bar{y}zw \vee x\bar{y}\bar{z}w \vee x\bar{y}\bar{z}\bar{w}, \\
 f_{12} &= xyz \vee xyw \vee x\bar{y}zw \vee x\bar{y}\bar{z}w \vee x\bar{y}\bar{z}\bar{w}, \\
 f_{13} &= xyz \vee x\bar{y}zw \vee x\bar{y}\bar{z}w \vee xyzw \vee xy\bar{z}w \vee x\bar{y}\bar{z}w \vee x\bar{y}\bar{z}\bar{w}, \\
 f_{14} &= xyw \vee x\bar{y}zw \vee x\bar{y}\bar{z}w \vee xyzw \vee xy\bar{z}w \vee x\bar{y}\bar{z}w \vee x\bar{y}\bar{z}\bar{w}.
 \end{aligned}$$

Here, too, the number of the function f corresponds to the number of the network on Fig. 7.

The advantages of any particular method depend on the specific case: on the network ^{and}, on the character and number of faults. For the purposes of control, it is convenient to construct the table in both manners.

In the compilation of the table it may be found that certain columns coincide identically. Thus, in the example under consideration here we have $f_7 = f_9$, $f_8 = f_{10}$, and $f_{13} = f_{14}$. The coincidence denotes that the corresponding faults are electrically undistinguishable or, if one of the columns is empty (always corresponds to the correct state) that the network contains excessive contacts. In the latter case, by removing these contacts we obtain a network equivalent to the initial one.

We note that the fact that certain fault functions coincide can be predicted directly from the network. In fact, if the permissible fault is a break in the contact, then, if two contacts are connected in series, it is impossible to establish which of these is broken.

Analogously, it is impossible to establish the shorting of a contact in the case of a parallel connection. It is interesting to ascertain a criterion that would permit finding the faults which are undistinguishable from the analysis of the network.

Thus, all the faults in the correct state are all broken up into classes such that the representatives of one class have identical columns, and the representatives of different classes have different columns. We shall henceforth deal with constructed classes, denoting them

the numbers of certain of their representatives.

2. Tests and Their Construction

Let \mathcal{M} be a set of functions $f(x_1, x_2, \dots, x_n)$, specified on and the same set E and assuming values from the set G (here n is the same for all the functions). We assume furthermore that all the functions from the set \mathcal{M} are pairwise different. Let furthermore there be fixed a certain subset \mathcal{N}^f (not ordered) pairs of functions of the set \mathcal{M} , where the pairs (f, f) are excluded.

Definition. A set $T \subset E$ is called a test (relative to $E, \mathcal{M}, \mathcal{N}^f$) if, no matter what pair of functions $(f, g) \in \mathcal{N}^f$, $f(x_1, x_2, \dots, x_n) \neq g(x_1, x_2, \dots, x_n)$ on the set T .

It is obvious that the concept of a test depends on the set \mathcal{N}^f . From the definition it follows that E is a test (trivial test).

Let us proceed now to describe the construction of tests. Let $T = \{e'_1, e'_2, \dots, e'_t\}$ be a certain test. Let us take $(f_i, f_j) \in \mathcal{N}^f$. Since T is a test, then there exists an assembly $e'_s \in E (1 \leq s \leq t)$ such that $f_i(e'_s) \neq f_j(e'_s)$. This assembly, consequently enters into the set E_{ij} -- the set of all the assemblies on which the functions f_i and f_j are different.

From this we have the following: T is the result of the selection from all the sets E_{ij} where $(f_i, f_j) \in \mathfrak{N}$

Attention should be called here to the fact that owing to the use of the "selection principle" (true, in a case of a finite set) in the formation of T , we obtain a cumbersome apparatus for the construction of tests.

To describe and construct tests it is convenient to use the apparatus of algebraic logic. In fact, let us write the set E_{ij} in the form of the formula

$$e_1 \& f_i(e_1) \neq f_j(e_1) \vee e_2 \& f_i(e_2) \neq f_j(e_2) \vee \dots \vee e_m \& f_i(e_m) \neq f_j(e_m) = e_1^{ij} \vee e_2^{ij} \vee \dots \vee e_{k_{ij}}^{ij}, \text{ i.e. } e_r^{ij} \in E = \{e_1, e_2, \dots, e_m\}.$$

We make up the expression

$$\prod_{(i,j) \in \mathfrak{N}} (e_1^{ij} \vee e_2^{ij} \vee \dots \vee e_{k_{ij}}^{ij}),$$

where under the sign \prod we understand the abbreviated notation for the expression

$$(\quad) \& (\quad) \& \dots \& (\quad).$$

The expression obtained is of the form $\prod \sum$. Applying the distributive law, and also the law of action with symbols e_k^{ij} as with the variables of algebraic logic, i.e., by putting $e_k \& e_k = e_k$ and $e_i \vee A \& e_i = e_i$,

we reduce the expression to the form $\sum \prod$, where the sum does not contain excessive terms. We can now formulate

the following proposition.

Theorem. The elements that enter into one term of $\sum \Pi$ generate a set which is an elementary test.

* A test T is called elementary, if any subset $T' \subset T$ is not a test.

The theorem follows from the fact that the term contains elements from each bracket $(e_1^{ij} \vee e_2^{ij} \vee \dots \dots \vee e_{k_{ij}}^{ij})$, where $(f_i, f_j) \in \mathcal{N}$.

Note. We see that the question of finding tests reduces to the construction of a set, which has in common with each subset in the expression of the form $\Pi \Sigma$ at least one element. Therefore the sets that have these properties with respect to the expression of the form will be called a test for the expression $\Pi \Sigma$.

We note that the transformation of $\Pi \Sigma$ to $\sum \Pi$ is cumbersome. This cumbersomeness reflects a more general set-theoretical fact, which states that under this kind of transformations it becomes frequently necessary to increase the cardinality (as in an Δ operation). The method of transformation will be investigated in greater detail in the next section. We shall indicate only one application of elementary tests here.

Definitions. The cardinality of the set T , which is a test, is called the length of the test. A test which has a minimal cardinality is called minimal.

It is obvious that all the minimal tests (of which there can be several) are found among the elementary tests. We shall henceforth be interested in minimal tests or in tests whose lengths are close to minimal.

Let \mathcal{M} be a set of fault functions. One can imagine that they are all reduced to a single table, as was already done (see Sec. 1). Let \mathcal{N} be a non-empty set of different unordered pairs of functions from \mathcal{M} . In our case \mathcal{N} will contain most frequently all such possible pairs. In the latter case the test is such a set, on which all the functions from \mathcal{M} are pairwise distinguishable. In other words, in order to detect a fault, it is enough to verify the network only for those sets, which are contained in the test. In the case when $T \neq E$, this verification is shorter than the verification with using all the assemblies. In addition, when $T \neq E$ there is no need of writing out the entire table of fault functions -- it is enough to know only that portion of the table, corresponding to the set T . By virtue of the foregoing, particular significance attaches to the problem of constructing minimal tests.

Note. The shorter the length of the test, the shorter the verification time of the network. However, this time can be reduced even further, by taking into account probability considerations. That is to say, once the network has been regulated, then the network is correct with the greatest probability; different faults are encountered with different probabilities. Taking furthermore into consideration that to detect a specific fault there is as a rule no need for "running through" the entire test (it is enough for this purpose to employ part of the assemblies), one can arrange the assemblies contained in the test in such an order that the mathematical expectation of the length of that portion of the test, which is necessary prior to disclosure of the fault, will be minimal.

In conclusion, we shall give examples of construction of minimal tests. The examples pertain to the network analyzed in Sec. 1. In example 1, the permissible faults are the closing of one contact, in example 2 are that of opening one contact. The assemblies e of the set E are denoted by integers, the binary arrangement of which, written from left to right, is identically equal to e .

The notation $0 \cdot 1|0 \vee 3 \vee 5 \vee 6$ denotes that the 0-th function differs from the 1-st function (see

table) in the 0, 3rd, 5th, and 6th assemblies.

Example 1.

Let us write out all the expressions of the form

$$e_1^{ij} \vee \dots \vee e_{k_{ij}}^{ij}$$

0 · 1	0 ∨ 3 ∨ 5 ∨ 6	1 · 2	0 ∨ 3 ∨ 5 ∨ 6 ∨ 9 ∨ 10 ∨ 12	2 · 3	12
0 · 2	9 ∨ 10 ∨ 12	1 · 3	0 ∨ 3 ∨ 5 ∨ 6 ∨ 9 ∨ 10	2 · 4	5 ∨ 6 ∨ 9 ∨ 10
0 · 3	9 ∨ 10	1 · 4	0 ∨ 3 ∨ 12	2 · 5	0 ∨ 3 ∨ 12
0 · 4	5 ∨ 6 ∨ 12	1 · 5	5 ∨ 6 ∨ 9 ∨ 10	2 · 6	5 ∨ 6 ∨ 9 ∨ 10 ∨ 12
0 · 5	0 ∨ 3 ∨ 9 ∨ 10	1 · 6	0 ∨ 3	2 · 7	0 ∨ 5 ∨ 10 ∨ 12
0 · 6	5 ∨ 6	1 · 7	3 ∨ 6 ∨ 9	2 · 8	3 ∨ 6 ∨ 9 ∨ 12
0 · 7	0 ∨ 5 ∨ 9	1 · 8	0 ∨ 5 ∨ 10	2 · 11	3 ∨ 5 ∨ 10 ∨ 12
0 · 8	3 ∨ 6 ∨ 10	1 · 11	0 ∨ 6 ∨ 9	2 · 12	0 ∨ 6 ∨ 9 ∨ 12
0 · 11	3 ∨ 5 ∨ 9	1 · 12	3 ∨ 5 ∨ 10	2 · 13	9 ∨ 10
0 · 12	9 ∨ 6 ∨ 10	1 · 13	0 ∨ 3 ∨ 5 ∨ 6 ∨ 12		
0 · 13	12				
3 · 4	5 ∨ 6 ∨ 9 ∨ 10 ∨ 12	4 · 5	0 ∨ 3 ∨ 5 ∨ 6 ∨ 9 ∨ 10 ∨ 12	5 · 6	0 ∨ 3 ∨ 5 ∨ 6 ∨ 9 ∨ 10
3 · 5	0 ∨ 3	4 · 6	12	5 · 7	3 ∨ 5 ∨ 10
3 · 6	5 ∨ 6 ∨ 9 ∨ 10	4 · 7	0 ∨ 6 ∨ 9 ∨ 12	5 · 8	0 ∨ 6 ∨ 9
3 · 7	6 ∨ 5 ∨ 10	4 · 8	3 ∨ 5 ∨ 10 ∨ 12	5 · 11	0 ∨ 5 ∨ 10
3 · 8	3 ∨ 6 ∨ 9	4 · 11	3 ∨ 6 ∨ 9 ∨ 12	5 · 12	3 ∨ 6 ∨ 9
3 · 11	3 ∨ 5 ∨ 10	4 · 12	0 ∨ 5 ∨ 10 ∨ 12	5 · 13	0 ∨ 3 ∨ 9 ∨ 10 ∨ 12
3 · 12	0 ∨ 6 ∨ 9	4 · 13	5 ∨ 6		
3 · 13	9 ∨ 10 ∨ 12				
6 · 7	0 ∨ 6 ∨ 9	7 · 8	0 ∨ 3 ∨ 5 ∨ 6 ∨ 9 ∨ 10	8 · 11	5 ∨ 6 ∨ 9 ∨ 10
6 · 8	3 ∨ 5 ∨ 10	7 · 11	0 ∨ 3	8 · 12	0 ∨ 3
6 · 11	3 ∨ 6 ∨ 9	7 · 12	5 ∨ 6 ∨ 9 ∨ 10	8 · 13	3 ∨ 6 ∨ 10 ∨ 12
6 · 12	0 ∨ 5 ∨ 10	7 · 13	0 ∨ 5 ∨ 9 ∨ 12		
6 · 13	5 ∨ 6 ∨ 12				
11 · 12	0 ∨ 3 ∨ 5 ∨ 6 ∨ 9 ∨ 10	12 · 13	0 ∨ 6 ∨ 10 ∨ 12		
11 · 13	3 ∨ 5 ∨ 9 ∨ 12				

The expression $\prod \sum$, after obvious simplifications,

becomes

$$\begin{aligned}
 \prod \sum &= (9 ∨ 10)(5 ∨ 6)(0 ∨ 5 ∨ 9)(3 ∨ 6 ∨ 10)(3 ∨ 5 ∨ 9)(0 ∨ 6 ∨ 10) \cdot 12 \cdot \\
 &\quad \cdot (0 ∨ 3)(3 ∨ 6 ∨ 9) \cdot (0 ∨ 5 ∨ 10)(0 ∨ 6 ∨ 9)(3 ∨ 5 ∨ 10) = \\
 &= (0 ∨ 3)(5 ∨ 6)(9 ∨ 10) \cdot 12 \cdot [(0 ∨ 5 ∨ 9)(3 ∨ 5 ∨ 9)] \cdot \\
 &\quad \cdot [(0 ∨ 5 ∨ 10)(3 ∨ 5 ∨ 10)] \cdot [(3 ∨ 6 ∨ 10)(0 ∨ 6 ∨ 10)] \cdot \\
 &\quad \cdot [(3 ∨ 6 ∨ 9)(0 ∨ 6 ∨ 9)] = (0 ∨ 3)(5 ∨ 6)(9 ∨ 10) \cdot 12 \cdot
 \end{aligned}$$

$$\begin{aligned} & \cdot [(0 \cdot 3 \vee 5 \vee 9)(0 \cdot 3 \vee 5 \vee 10)] \cdot [(0 \cdot 3 \vee 6 \vee 9)(0 \cdot 3 \vee 6 \vee 10)] = \\ & = (0 \vee 3)(5 \vee 6)(9 \vee 10) \cdot 12 \cdot [(0 \cdot 3 \vee 5 \vee 9 \cdot 10)(0 \cdot 3 \vee 6 \vee 9 \cdot 10)] = (0 \vee 3) \cdot \\ & \quad \cdot (5 \vee 6)(9 \vee 10) \cdot 12 \cdot (0 \cdot 3 \vee 5 \cdot 6 \vee 9 \cdot 10) \end{aligned}$$

By opening up the brackets we obtain

$$\begin{aligned} \Sigma II = & 0 \cdot 3 \cdot 5 \cdot 9 \cdot 12 \vee 0 \cdot 3 \cdot 5 \cdot 10 \cdot 12 \vee 0 \cdot 3 \cdot 6 \cdot 10 \cdot 12 \vee 0 \cdot 3 \cdot 6 \cdot 9 \cdot 12 \vee \\ & \vee 0 \cdot 5 \cdot 6 \cdot 9 \cdot 12 \vee 0 \cdot 5 \cdot 6 \cdot 10 \cdot 12 \vee 3 \cdot 5 \cdot 6 \cdot 9 \cdot 12 \vee 3 \cdot 5 \cdot 6 \cdot 10 \cdot 12 \vee \\ & \vee 0 \cdot 5 \cdot 9 \cdot 10 \cdot 12 \vee 0 \cdot 6 \cdot 9 \cdot 10 \cdot 12 \vee 3 \cdot 5 \cdot 9 \cdot 10 \cdot 12 \vee 3 \cdot 6 \cdot 9 \cdot 10 \cdot 12. \end{aligned}$$

Each term defines a minimal test.

Example 2.

Let us write out again all the expression of the form

		$e_1^{ij} \vee \dots \vee e_{k_{ij}}^{ij}$
0 \cdot 1'	$8 \vee 11 \vee 13 \vee 14 \vee 15$	1' \cdot 2' \vee 4 \vee 7 \vee 8 \vee 11 \vee 13 \vee 14 \vee 15
0 \cdot 2'	$1 \vee 2 \vee 4 \vee 7$	1' \cdot 3' \vee 8 \vee 11
0 \cdot 3'	$13 \vee 14 \vee 15$	1' \cdot 4' \vee 13 \vee 14 \vee 15
0 \cdot 4'	$8 \vee 11$	1' \cdot 5' \vee 4 \vee 7 \vee 8 \vee 11 \vee 13 \vee 14 \vee 15
0 \cdot 5'	$4 \vee 7$	1' \cdot 6' \vee 1 \vee 2 \vee 8 \vee 11 \vee 13 \vee 14 \vee 15
0 \cdot 6'	$1 \vee 2$	1' \cdot 7' \vee 7 \vee 8 \vee 13 \vee 14 \vee 15
0 \cdot 7'	$7 \vee 11$	1' \cdot 8' \vee 4 \vee 11 \vee 13 \vee 14 \vee 15
0 \cdot 8'	$4 \vee 8$	1' \cdot 9' \vee 2 \vee 8 \vee 11 \vee 13 \vee 14 \vee 15
0 \cdot 9'	2	1' \cdot 10' \vee 1 \vee 8 \vee 11 \vee 13 \vee 14 \vee 15
0 \cdot 10'	1	1' \cdot 11' \vee 2 \vee 4 \vee 11 \vee 13 \vee 14 \vee 15
0 \cdot 11'	$2 \vee 4 \vee 8$	1' \cdot 12' \vee 1 \vee 7 \vee 8 \vee 13 \vee 14 \vee 15
0 \cdot 12'	$1 \vee 7 \vee 11$	1' \cdot 13' \vee 8 \vee 11 \vee 14 \vee 15
0 \cdot 13'	13	1' \cdot 14' \vee 8 \vee 11 \vee 13 \vee 15
0 \cdot 14'	14	

2', 3'	1\2\4\7\13\14\15	3', 4'	8\11\13\14\15	4', 5'	4\7\8\11
2', 4'	1\2\4\7\8\11	3', 5'	4\7\13\14\15	4', 6'	1\2\8\11
2', 5'	1\3	3', 6'	1\2\13\14\15	4', 7'	7\8
2', 6'	4\7	3', 7'	7\11\13\14\15	4', 8'	4\11
2', 7'	1\2\4\7\11	3', 8'	4\8\13\14\15	4', 9'	2\8\11
2', 8'	1\2\7\8	3', 9'	2\13\14\15	4', 10'	1\8\11
2', 9'	1\4\7	3', 10'	1\13\14\15	4', 11'	2\4\11
2', 10'	2\4\7	3', 11'	2\4\8\13\14\15	4', 12'	1\7\8
2', 11'	1\7\8	3', 12'	1\7\11\13\14\15	4', 13'	8\11\13
2', 12'	2\4\11	3', 13'	14\15	4', 14'	8\11\14
2', 13'	1\2\4\7\13	3', 14'	13\15		
2', 14'	1\2\4\7\14				
5', 6'	1\2\4\7	6', 7'	1\2\7\11	7', 8'	4\7\8\11
5', 7'	4\11	6', 8'	1\2\4\8	7', 9'	2\7\11
5', 8'	7\8	6', 9'	1	7', 10'	1\7\11
5', 9'	2\4\7	6', 10'	2	7', 11'	2\4\7\8\11
5', 10'	1\4\7	6', 11'	1\4\8	7', 12'	1
5', 11'	2\7\8	6', 12'	2\7\11	7', 13'	7\11\13
5', 12'	1\4\11	6', 13'	1\2\13	7', 14'	7\11\14
5', 13'	4\7\13	6', 14'	1\2\14		
5', 14'	4\7\14				
8', 9'	2\4\8	9', 10'	1\2	10', 11'	1\2\4\8
8', 10'	1\4\8	9', 11'	4\8	10', 12'	7\11
8', 11'	2	9', 12'	1\2\7\11	10', 13'	1\13
8', 12'	1\4\7\8\11	9', 13'	2\13	10', 14'	1\14
8', 13'	4\8\13	9', 14'	2\14		
8', 14'	4\8\14				
11', 12'	1\2\4\7\8\11	12', 13'	1\7\11\13	13', 14'	13\14
11', 13'	2\4\8\13	12', 14'	1\7\11\14		
11', 14'	2\4\8\14				

After obvious simplifications, we can write for $\Pi\Sigma$ the following:

$$\Pi\Sigma = 1 \cdot 2 \cdot 13 \cdot 14 [(4 \vee 11)(7 \vee 11)(8 \vee 11)] [(4 \vee 8)(7 \vee 8)(4 \vee 7)] = \\ = 1 \cdot 2 \cdot 13 \cdot 14 (11 \vee 4 \cdot 7 \cdot 8)(8 \vee 4 \cdot 7)(4 \vee 7).$$

Transforming this expression, we obtain

$$\Sigma\Pi = 1 \cdot 2 \cdot 4 \cdot 8 \cdot 11 \cdot 13 \cdot 14 \vee 1 \cdot 2 \cdot 4 \cdot 7 \cdot 8 \cdot 13 \cdot 14 \vee 1 \cdot 2 \cdot 7 \cdot 8 \cdot 11 \cdot 13 \cdot 14 \vee \\ \vee 1 \cdot 2 \cdot 4 \cdot 7 \cdot 11 \cdot 13 \cdot 14.$$

Each term will define a minimal test.

3. Certain Rules for the Construction of Tests

We have already seen that the construction of tests reduces to the construction of an expression of the type $\sum\Pi$. In the general case, to construct a $\sum\Pi$ it is necessary first to obtain the expression $\Pi\Sigma$ and then convert it to the form $\sum\Pi$. Both these stages are exceedingly laborious. By virtue of these circumstances, it becomes practically impossible to construct minimal tests for arbitrary networks, using an algorithm that does not take into account the peculiarities of the structure of the networks, which realize functions of six or more variables.

It must be noted that a direct expanding of the brackets even in a whole series of relatively simple problems leads to a very large number of terms; thus, in the opening of the brackets in example 1

of Sec. 2, one obtains more than a million of terms. However, the final result contains, as a rule, much fewer terms. In this connection, the question arises of finding simpler ^{schemes}, when it is possible: 1) to construct a $\Pi\Sigma$ starting with a table; 2) to convert the $\Pi\Sigma$ into $\Sigma\Pi$, bypassing the direct opening of the brackets with a consequent "reduction of similars," and 3) in the case of construction of a minimal test or any one fully definite test for the elimination of the transformation of $\Pi\Sigma$ into $\Sigma\Pi$.

In the present section we shall formulate briefly these rules.

I. Rules of Construction of $\Pi\Sigma$. 1. In the table of fault functions we discard the rows that consist either entirely of 0's or entirely of 1's, and also the corresponding assemblies.

2. In the case when the table contains identical rows, we discard all of them together with the corresponding assemblies, leaving one representative of each.

We shall disregard from now on the discarded assemblies, assuming that the functions are not defined on them.

3. We choose all the assemblies that have that property, that for each of these there are at least

two functions which assume on these assemblies different values, and on the remaining (which remain after I_1 and I_2) identical values. The resultant assemblies exhaust all the one-term factors in the $\prod \Sigma$ expression.

4. Let $e_{i_1}, e_{i_2}, \dots, e_{i_s}$ be one-term assemblies, obtained according to item 3. We remove from the set all the pairs of functions (f_i, f_j) for which there exists an assembly e_{i_k} ($1 \leq k \leq s$) such that $f_i(e_{i_k}) \neq f_j(e_{i_k})$. The resultant set will be denoted by \mathcal{N}' . It is obvious that the construction of a test in a case when a set of pairs \mathcal{N}' is fixed is simpler than for the set of pairs $\mathcal{N} < \mathcal{N}'$. Let us assume that $\prod \Sigma'$ corresponds to the set \mathcal{N}' . Then, obviously, we have $\prod \Sigma = e_{i_1} e_{i_2} \dots e_{i_s} \prod \Sigma'$.

In practice it is more convenient to proceed as follows: using the sets $e_{i_1}, e_{i_2}, \dots, e_{i_s}$ one breaks up the set \mathcal{N} into classes in such a way, that the representatives of different classes on a certain assembly e_{i_k} ($1 \leq k \leq s$) assume different values, and the representative of one class on each of the considered assemblies assume one and the same value.

Next, for each pair of functions $(f_i, f_j) \in \mathcal{N}$ and such that the functions f_i and f_j enter into one class, consequently, $(f_i, f_j) \in \mathcal{N}'$, one constructs the set E_{ij} , etc.

5. Using the rule that $A(A \vee B) = A$, we cross out in the $\Pi\Sigma$ expression the excessive factors. It should be noted here that when item 4 is satisfied, the factors which are absorbed by the terms $e_{i1}, e_{i2}, \dots, e_{is}$ are automatically discarded.

II. Rules of Transformation of $\Pi\Sigma$ into $\Sigma\Pi$.

1. Algebraic Method. Using the distributive law, we carry out the multiplication of the brackets

$$(A \vee B)C = AC \vee BC.$$

This is followed by further transformations, in which the identities

$$A \cdot A = A, AB = BA, A \vee B = B \vee A, A \vee AB = A.$$

are taken into account. It becomes frequently convenient here first to group the factors in a suitable manner.

2. The geometric method is based on the relation

$$\Pi\Sigma e_{ij} = \overline{\Sigma\Pi e_{ij}}.$$

In other words, the result of the operation $\Pi\Sigma$ is the complement to the result of the operation $\Sigma\Pi$ on the complement. Thus, it becomes possible to obtain the expression of interest to us by using the supplementary operation to the operation $\Pi\Sigma$ /4/. For this purpose, we consider a "sieve," which has the following form: in a rectangle parallel to the base one draws a total of m straight lines, where m equals

the number of different assemblies e_1, e_2, \dots, e_m of the function $f(x_1, x_2, \dots, x_n)$; let us assume that these are numbered as shown in Fig. 8. Next, we separate the segment 1 into two equal parts, segment 2 into four parts, etc.; finally we divide segment m into 2^m equal parts.

From segment 1 we remove the first half, we remove the 1-st and 3-rd quarter of segment 2, we remove the 1-st, 3-rd, 5-th, and 7-th eighths from segment 3, etc. The discarded part of the i -th segment of the sieve is set in correspondence with the assembly e_j and the undiscarded part is set in correspondence with the assembly \bar{e}_j ($1 \leq i \leq m$). To each product $\prod \bar{e}_{ij}$ we set in correspondence a part of the sieve; for this purpose, all the factors from the product $\prod \bar{e}_{ij}$ are mentally projected on the segment in which is located the factor of the highest rank in the given product, and we take their intersection. The resultant part of the sieve will be called sparated. By carrying out such an operation with each term of $\sum \prod \bar{e}_{ij}$ we separate from the sieve a certain set of segments. Let us divide the base of the triangle int 2^m parts. To each part of the subdivision, which is not contained in the projection on the base of the separated part of the sieve, we assign an index defined as follows: from an internal point of the given part we draw a perpendicular and take

the difference between m and the number of points of intersection of the perpendicular with the sieve, or, what is the same, we count the number of horizontal lines on which the perpendicular does not intersect with the sieve. (See reference /2/.)

It is easy to see that each part of the breakdown of the base, in which an index is defined, corresponds to an elementary test consisting of assemblies corresponding to all those segments, with which the perpendicular drawn from the internal point of the considered part does not intersect. It is furthermore evident that the length of the elementary test, corresponding to the given part of the breakdown is equal to its index.

III. Rules of Construction of a Minimal Test. In the construction of a minimal test it is necessary to choose a certain term from the $\sum \pi$, and therefore, in many cases, there is no need for carrying out a complete transformation from $\pi \sum$ to $\sum \pi$. This is aided by the following two rules.

1. If the product $\pi \sum$ breaks up into groups such that the different groups do not have identical assemblies, then in order to obtain a minimal test it is sufficient to construct a minimal test for each group and to take their joining.

In the case when the permissible faults are either

the closing of one contact or the opening of one contact it is obvious that the minimal test breaks down into two nonintersecting tests: the first is minimal for closing in one contact and the other is minimal for opening in one contact. In other words, in this case the $\mathbb{T}\Sigma$ always breaks down at least into two groups without common assembly. This follows from the fact that in the case under consideration the fault functions corresponding to closing do not differ from the initial function on those assemblies in which $f(e) = 1$, and correspondingly the fault functions corresponding to open ^{circuits} do not differ from the initial function on those assemblies where $f(e) = 0$.

2. Let the expression $\mathbb{T}\Sigma$ have the form

$$(e_i \vee e_j)(A_1 \vee e_i e_j B_1)(A_2 \vee e_i e_j B_2) \dots (A_\tau \vee e_i e_j B_\tau) C,$$

where $A_1, B_1, A_2, B_2, \dots, A_\tau, B_\tau$ do not contain the assemblies e_i and e_j , and the term C (which has the form $\mathbb{T}\Sigma$) does not contain the assembly e_i (there may not be any brackets in A and B). It is obvious that in the minimal test, owing to the factor $(e_i \vee e_j)$, there should be contained either e_i or e_j ; here it is more convenient to take first e_j , since both e_i and e_j enter symmetrically in all the factors, with the exception of C , while e_j may also enter in C .

To prove this we note that if the expression $\Pi\Sigma_2$ is obtained from the expression $\Pi\Sigma_1$ by crossing out a certain number of conjunctive terms, then to each test T_1 of the expression $\Pi\Sigma_1$ there corresponds a test T_2 of the expression $\Pi\Sigma_2$, with $T_2 \subset T_1$ (in such a crossing-out, the length of the test can only decrease).

Let us consider two cases:

a) the element e_i is chosen; when e_i is crossed out, $\Pi\Sigma$ becomes

$$\Pi\Sigma_1 = (A_1 \vee e_i B_1) (A_2 \vee e_i B_2) \dots (A_r \vee e_i B_r) C$$

b) the element e_j is chosen; when e_j is crossed out, $\Pi\Sigma$ becomes

$$\Pi\Sigma_2 = (A_1 \vee e_j B_1) (A_2 \vee e_j B_2) \dots (A_r \vee e_j B_r) C$$

If we now replace e_i by e_j , then the expression $\Pi\Sigma_2$ will be the result of crossing out of a certain number of conjunctive elements from the expression and therefore in case b) the test can only be less.

3. Let $\Pi\Sigma$ be broken up into groups of factors, with $e_{i1}, e_{i2}, \dots, e_{it}$ being the minimal test of the first group, and e_i^0 being the minimal test of the second group; then a) if $e_{i1}, e_{i2}, \dots, e_{it}$ is the test for the second group, then $e_{i1}, e_{i2}, \dots, e_{it}$ is a minimal test for the entire product; b) if any minimal test of the first group is not a test for the second group, then $e_i^0, e_{i1}, \dots, e_{it}$ is a minimal test

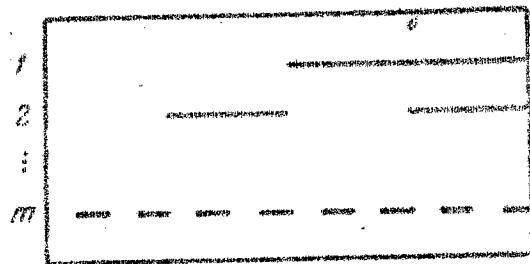


Fig. 8

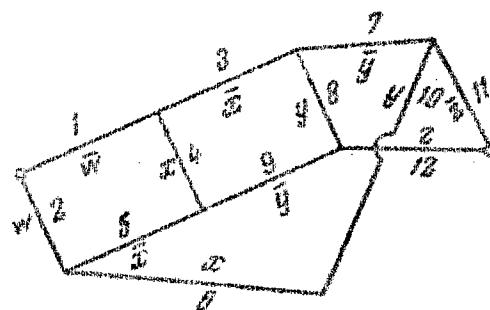


Fig. 9

for the entire product.

The given rules do not exhaust other possible measures that facilitate the compilation of the test. To the contrary, searches for effective rules make up one of the important problems in test theory.

Certain other measures, which permit a simpler construction of the test, are described in the following chapter.

Example. In conclusion let us give an example of the construction of a minimal test by the two methods, in the case when the permissible faults are the opening ^[breaking] or the closing ^[shorting] of a single contact. Taking into account rule III₁, it is enough to construct tests for the case of closing and opening separately. The first method illustrates the rules I₃, I₄, I₅, III₁, III₂, and III₃, whereas the second explains the geometric method of constructing tests.

Let us consider the network shown in Fig. 9, which realizes the function

$$f_0(x, y, z, w) = \bar{x}\bar{y}zw \vee x\bar{y}zw \vee xy\bar{z}w \vee x\bar{y}zw \vee xy\bar{z}w.$$

Figs. 10 and 11 show the states of the networks for different values of the assemblies; the asterisks mark those contacts, the faults of which (closing in Fig. 10 and opening in Fig. 11) convert the network to the opposite position (in the sense of admittance).

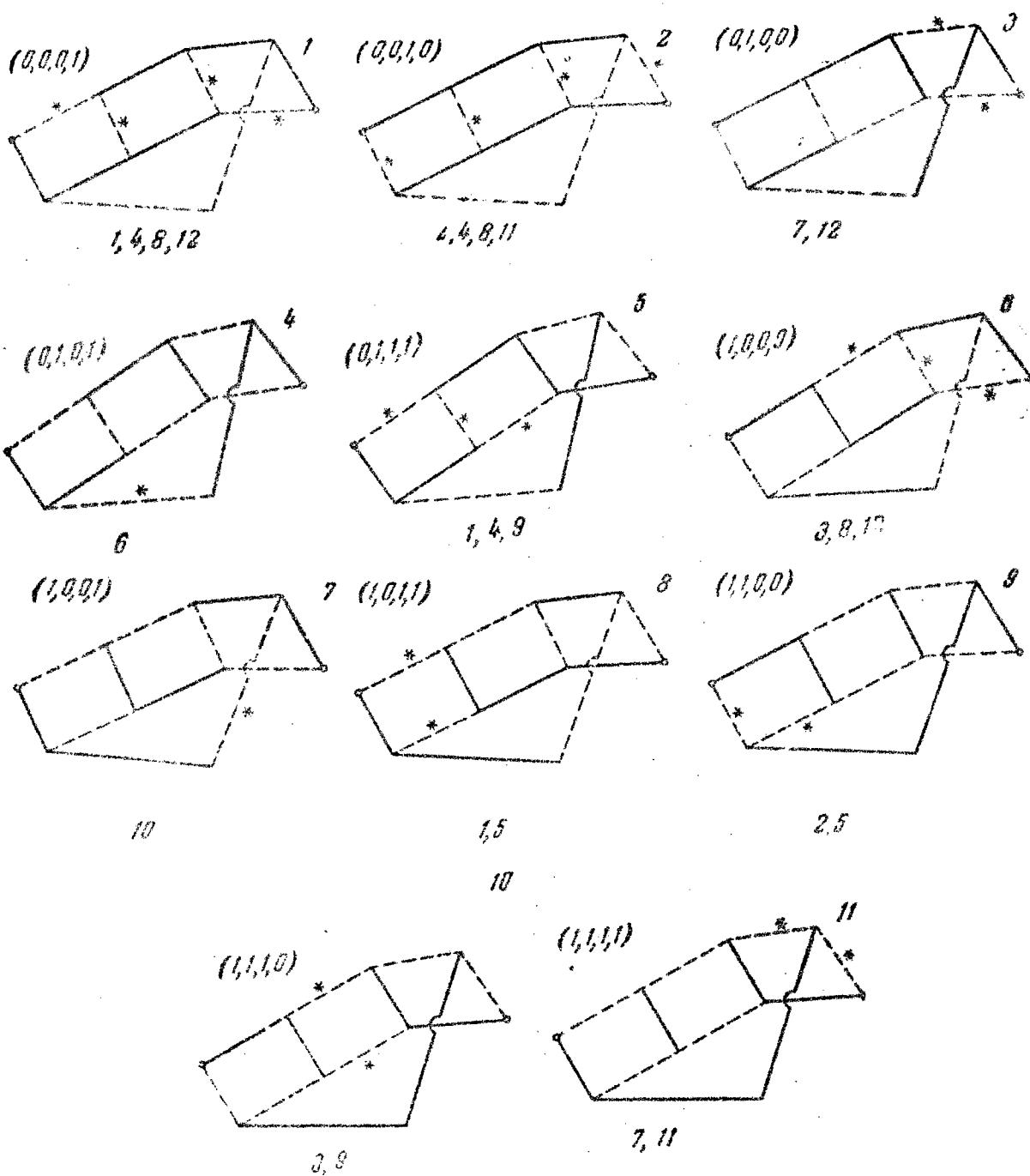


Fig. 10

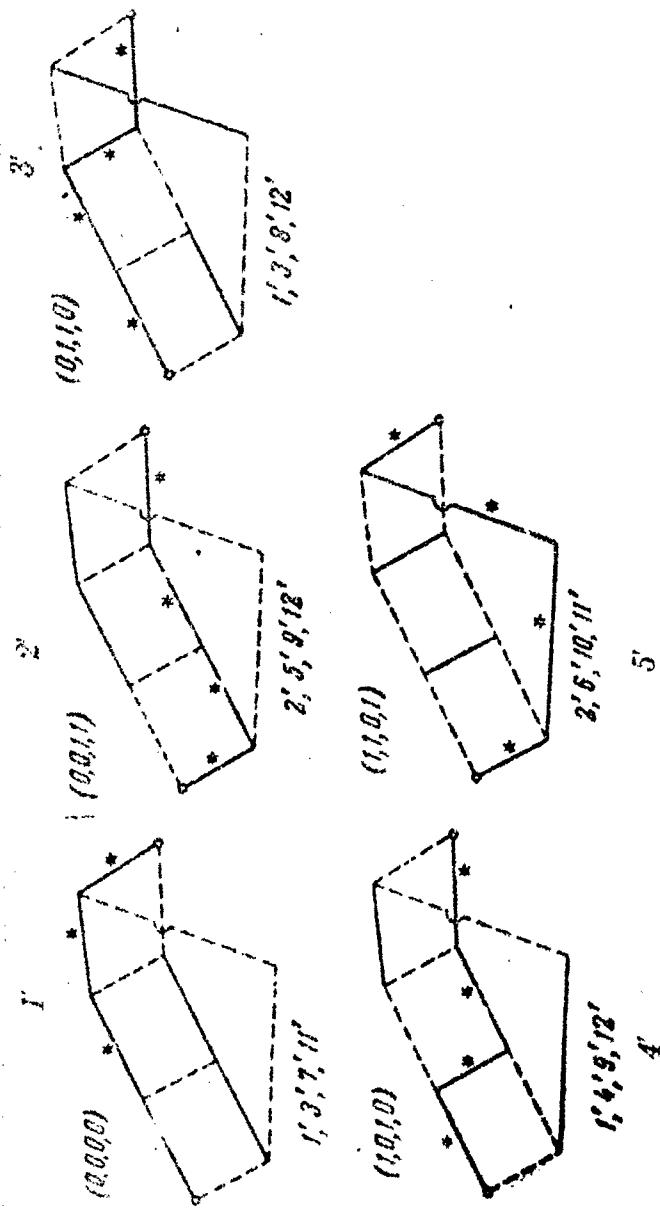


Fig. 11

The states of the networks for different values of the assemblies, shown in Figs. 10 and 11, can be gathered in a single table of fault functions (Table 2)

Table 2

	0	1	2	3	4	5	6	7	8	9	10	11	12	1' 2'	3' 4'	5' 6'	7' 8'	9' 10'	11' 12'
(0, 0, 0, 1)	0	1		1			1			1									
(0, 0, 1, 0)	0		1	1				1			1								
(0, 1, 0, 0)	0						1					1							
+	(0, 1, 0, 1)	0					1												
(0, 1, 1, 1)	0	1			1					1									
(1, 0, 0, 0)	0		1					1				1							
+	(1, 0, 0, 1)	0								1									
(1, 0, 1, 1)	0	1				1													
(1, 1, 0, 0)	0		1				1												
(1, 1, 1, 0)	0			1						1									
(1, 1, 1, 1)	0					1					1								
+	(0, 0, 0, 0)	1										0	0		0		0		0
+	(0, 0, 1, 1)	1										0	0		0		0		0
+	(0, 1, 1, 0)	1										0	0		0		0		0
+	(1, 0, 1, 0)	1										0	0		0		0		0
+	(1, 1, 0, 1)	1										0	0		0		0		0

$$f_{6'} = f_{10'}$$

Let us consider first the cases of closing (Fig. 10).

We see that the single-term factors will be assemblies 5 and 9. They represent the following breakdown of the fault functions

$$5 \left\{ \begin{array}{l} 6 \\ 0, 1, 2, 3, 4, 5, 7, 8, 9, 10, 11, 12 \end{array} \right.$$

$$9 \left\{ \begin{array}{l} 10 \\ 0, 1, 2, 3, 4, 5, 7, 8, 9, 11, 12 \end{array} \right.$$

0 · 1	$1 \vee 7 \vee 11$	1 · 2	$1 \vee 2 \vee 7 \vee 11 \vee 12$	2 · 3	$2 \vee 8 \vee 12 \vee 14$
0 · 2	$2 \vee 12$	1 · 3	$1 \vee 7 \vee 8 \vee 11 \vee 14$	2 · 4	$1 \vee 7 \vee 12$
0 · 3	$8 \vee 14$	1 · 4	$2 \vee 11$	2 · 5	$2 \vee 11$
0 · 4	$1 \vee 2 \vee 7$	1 · 5	$1 \vee 7 \vee 12$	2 · 7	$2 \vee 4 \vee 12 \vee 15$
0 · 5	$11 \vee 12$	1 · 7	$1 \vee 4 \vee 7 \vee 11 \vee 15$	2 · 8	$1 \vee 8 \vee 12$
0 · 7	$4 \vee 15$	1 · 8	$2 \vee 7 \vee 8 \vee 11$	2 · 9	$2 \vee 7 \vee 12 \vee 14$
0 · 8	$1 \vee 2 \vee 8$	1 · 9	$1 \vee 11 \vee 14$	2 · 11	$12 \vee 15$
0 · 9	$7 \vee 14$	1 · 11	$1 \vee 2 \vee 7 \vee 11 \vee 15$	2 · 12	$1 \vee 2 \vee 4 \vee 8 \vee 12$
0 · 11	$2 \vee 15$	1 · 12	$4 \vee 7 \vee 8 \vee 11$		
0 · 12	$1 \vee 4 \vee 8$				
3 · 4	$1 \vee 2 \vee 7 \vee 8 \vee 14$	4 · 5	$1 \vee 2 \vee 7 \vee 11 \vee 12$	5 · 7	$4 \vee 11 \vee 12 \vee 15$
3 · 5	$8 \vee 11 \vee 12 \vee 14$	4 · 7	$1 \vee 2 \vee 4 \vee 7 \vee 15$	5 · 8	$1 \vee 2 \vee 8 \vee 11 \vee 12$
3 · 7	$4 \vee 8 \vee 14 \vee 15$	4 · 8	$7 \vee 8$	5 · 9	$7 \vee 11 \vee 12 \vee 14$
3 · 8	$1 \vee 2 \vee 14$	4 · 9	$1 \vee 2 \vee 14$	5 · 11	$2 \vee 11 \vee 12 \vee 15$
3 · 9	$7 \vee 8$	4 · 11	$1 \vee 7 \vee 15$	5 · 12	$1 \vee 4 \vee 8 \vee 11 \vee 12$
3 · 11	$2 \vee 8 \vee 14 \vee 15$	4 · 12	$2 \vee 4 \vee 7 \vee 8$		
3 · 12	$1 \vee 4 \vee 14$				
7 · 8	$1 \vee 2 \vee 4 \vee 8 \vee 15$	8 · 9	$1 \vee 2 \vee 7 \vee 8 \vee 14$	9 · 11	$2 \vee 7 \vee 14 \vee 15$
7 · 9	$4 \vee 7 \vee 14 \vee 15$	8 · 11	$1 \vee 8 \vee 15$	9 · 12	$1 \vee 4 \vee 7 \vee 8 \vee 14$
7 · 11	$2 \vee 4$	8 · 12	$2 \vee 4$		
7 · 12	$1 \vee 8 \vee 15$				
11 · 12	$1 \vee 2 \vee 4 \vee 8 \vee 15$				

Thus, in the case of closing we obtain (taking I_5 into account) the following expression for $\Pi \leq$:

$$\begin{aligned} \Pi \Sigma = & 5 \cdot 9 (2 \vee 12) (8 \vee 14) (11 \vee 12) (4 \vee 15) (7 \vee 14) (2 \vee 15) (2 \vee 11) \cdot \\ & \cdot (12 \vee 15) (7 \vee 8) (2 \vee 4) (1 \vee 7 \vee 11) (1 \vee 2 \vee 7) (1 \vee 2 \vee 8) (1 \vee 4 \vee 8) \cdot \\ & \cdot (1 \vee 7 \vee 12) (1 \vee 11 \vee 14) (1 \vee 8 \vee 12) (1 \vee 2 \vee 14) (1 \vee 4 \vee 14) (1 \vee 7 \vee 15) \cdot \\ & \cdot (1 \vee 8 \vee 15) \end{aligned}$$

Let us now proceed to the construction of the minimal test.

First Method. Since

$$\begin{aligned}(11 \vee 2)(11 \vee 12) &= 11 \vee 2 \cdot 12, \\ (15 \vee 2)(15 \vee 12) &= 15 \vee 2 \cdot 12, \\ (1 \vee 7 \vee 2)(1 \vee 7 \vee 12) &= 1 \vee 7 \vee 2 \cdot 12, \\ (1 \vee 8 \vee 2)(1 \vee 8 \vee 12) &= 1 \vee 8 \vee 2 \cdot 12,\end{aligned}$$

we obtain

$$\begin{aligned}\Pi\Sigma &= 5 \cdot 9 ((2 \vee 12)(11 \vee 2 \cdot 12)(15 \vee 2 \cdot 12)(1 \vee 7 \vee 2 \cdot 12)(1 \vee 8 \vee 2 \cdot 12)) \\ &\quad \times ((2 \vee 4)(1 \vee 2 \vee 14)(8 \vee 14)(4 \vee 15)(7 \vee 14)(7 \vee 8)(1 \vee 7 \vee 11)) \\ &\quad \times (1 \vee 4 \vee 8)(1 \vee 11 \vee 14)(1 \vee 4 \vee 14)(1 \vee 7 \vee 15)(1 \vee 8 \vee 15)).\end{aligned}$$

Since 2 and 12 enter in the first curly bracket symmetrically, and only 2 enters into the second bracket, then according to III_2 the minimal test should contain 2.

In addition, according to III_1 , the minimal test contains 5 and 9. After choosing the indicated elements we remove from the $\Pi\Sigma$ all the factors containing these elements as terms. We obtain

$$\begin{aligned}\Pi\Sigma' &= (11 \vee 12)(15 \vee 12)(1 \vee 7 \vee 12)(1 \vee 8 \vee 12)(8 \vee 14)(4 \vee 15) \cdot \\ &\quad \cdot (7 \vee 14)(7 \vee 8)(1 \vee 7 \vee 11)(1 \vee 4 \vee 8)(1 \vee 11 \vee 14)(1 \vee 4 \vee 14) \cdot \\ &\quad \cdot (1 \vee 7 \vee 15)(1 \vee 8 \vee 15).\end{aligned}$$

Taking into consideration that

$$\begin{aligned}(7 \vee 8)(8 \vee 14)(7 \vee 14) &= 7 \cdot 8 \vee 7 \cdot 14 \vee 8 \cdot 14, \\ (1 \vee 7 \vee 12)(1 \vee 7 \vee 15)(1 \vee 8 \vee 12)(1 \vee 8 \vee 15) &= 1 \vee 7 \cdot 8 \vee 12 \cdot 15, \\ (1 \vee 4 \vee 8)(1 \vee 4 \vee 14) &= 1 \vee 4 \vee 8 \cdot 14, \\ (1 \vee 11 \vee 7)(1 \vee 11 \vee 14) &= 1 \vee 11 \vee 7 \cdot 14,\end{aligned}$$

we obtain

$$\Pi\Sigma' = \{((11 \vee 12)(15 \vee 12)(4 \vee 15)) [7 \cdot 8 \vee 7 \cdot 14 \vee 8 \cdot 14]\} \cdot \\ \cdot \{((1 \vee 7 \cdot 8 \vee 12 \cdot 15)(1 \vee 4 \vee 8 \cdot 14)(1 \vee 11 \vee 7 \cdot 14)\}.$$

The second curly bracket has a minimal test 1. The first curly bracket breaks down into two factors without common elements, and therefore its minimal test is a combination of the minimal tests for these factors (III₁). The first factor has the following minimal tests: 4, 12; 15, 11; and 15 12; the second factor has the following minimal tests: 7, 8; 7, 14; and 8, 14.

Thus, the first curly bracket has 9 minimal tests; and none of these is a test for the second curly bracket. Hence by III₃ the minimal test for $\Pi\Sigma'$ is the joining of any minimal test for the first curly bracket, let us say 11, 15, 7, 8, and the minimal test for the second curly bracket, i.e. 1.

We have the following minimal test

$$1, 2, 5, 7, 8, 9, 11 \vee 15.$$

In the case of opening (see Fig. 11) we have the following one-term factors: 0, 3, 6, 10, and 13. These assemblies carry out the complete breakdown of all the fault functions for openings. In fact

$$0 \begin{cases} 0, 2, 4, 5, 8, 9, 10, 12 \\ 1, 3, 7, 11 \end{cases} \quad 3 \begin{cases} 0, 4, 8, 10 \\ 2, 5, 9, 12 \end{cases}$$

$$6 \left\{ \begin{matrix} 7' \\ 1' \end{matrix} \right. \left\{ \begin{matrix} 11' \\ 3' \end{matrix} \right. \left\{ \begin{matrix} 2' \\ 42' \end{matrix} \right. \left\{ \begin{matrix} 5' \\ 9' \end{matrix} \right. \left\{ \begin{matrix} 0' \\ 8' \end{matrix} \right. \left\{ \begin{matrix} 4' \\ 10' \end{matrix} \right.$$

$$10 \left\{ \begin{matrix} 3' \\ 1' \end{matrix} \right. \left\{ \begin{matrix} 0' \\ 4' \end{matrix} \right. \left\{ \begin{matrix} 10' \\ 9' \end{matrix} \right. \left\{ \begin{matrix} 2' \\ 5' \end{matrix} \right. \left\{ \begin{matrix} 5' \\ 8' \end{matrix} \right. \left\{ \begin{matrix} 0' \\ 10' \end{matrix} \right. \left\{ \begin{matrix} 7' \\ 11' \end{matrix} \right.$$

From this we have

$$\Pi\Sigma = 0 \cdot 3 \cdot 6 \cdot 10 \cdot 13.$$

Consequently 0, 3, 6, 10, and 13 is the only minimal test.

Note. The process of constructing a test usually contains a large number of calculations, and therefore it is sensible to verify in the end whether the constructed set of assemblies is actually a test. For this purpose, using the constructed assemblies, one breaks down the fault functions: if the breakdown is complete, i.e., for each pair $(f_i, f_j) \in \mathcal{Y}_L$ there exists in the constructed set an assembly such that $f_i(e) \neq f_j(e)$, we have a test. In the opposite case the set is not a test. An example of such a verification was given in the example considered.

Second Method. Starting out with the expression for $\Pi\Sigma$ (see p. 291 [of source]) and using the description Π_2 , we obtain the sieve shown in Fig. 12. For the purpose of economy of space, the sieve is cut up into four parts. To restore the initial picture it is necessary to consider each lower rectangle as a

1
2
4
7
8
11
12
14
15

83 39 7 87 78 87 7 76

1
2
4
7
8
11
12
14

8 7 7 7

1
2
4
7
8
11
12
14
15

87 57 6 76 7 6 7

1
2
4
7
8
11
12
14
15

Fig 12 (1st half)

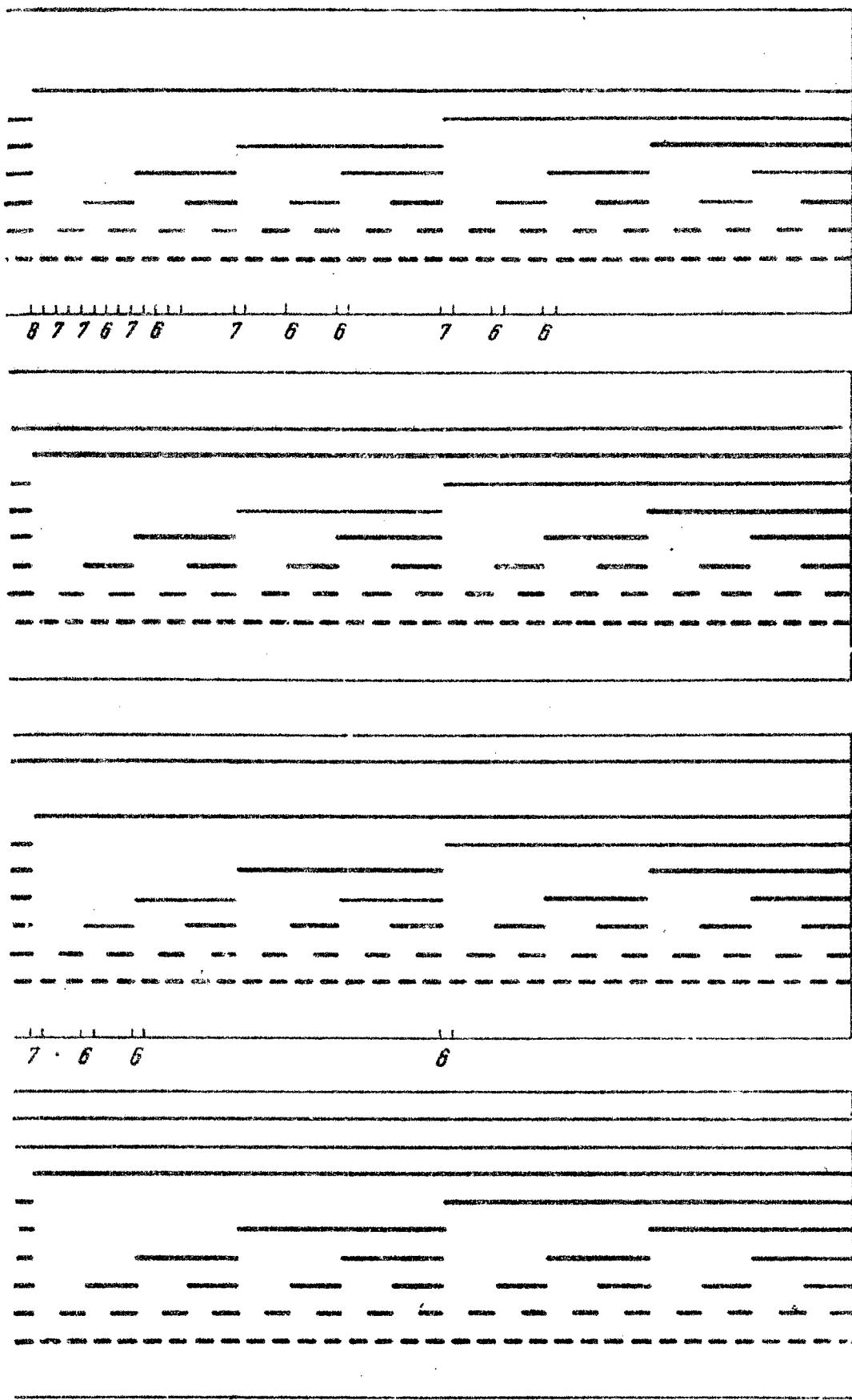


Fig. 1d (2nd half)

direct continuation of the rectangle located above it. In Fig. 12 the heavy dotted line and the heavy segments indicate the separated subset of the sieve.

IV. Construction of Sufficiently Simple Tests.

One can be satisfied with the construction of not a minimal test, but a test which is sufficiently good in that sense that its length does not exceed too strongly the length of the minimal test. This question has a greater significance if the construction of the indicated test is essentially simpler than the construction of the minimal test.

We shall now indicate how, starting out with the $\prod \Sigma$ expression, one can rather simply construct a test which is quite satisfactory. However, the question of how much this test differs from the minimal one remains moot.

The construction of the test reduces to the following.

1. In the $\prod \Sigma$ expression we choose the element e_{i_1} , which is encountered in the largest number of factors (if there are a few of them, we take anyone of these).

2. We cross out from the $\prod \Sigma$ expression the factors which contain the chosen element e_{i_1} and obtain $\prod \Sigma'$.

If $\Pi\Sigma'$ is empty, then the test is e_{i_1} . If it is not empty, then applying items 1 and 2 to the expression, we obtain e_{i_2} , etc. Thus, we arrive at a test $e_{i_1}, e_{i_2}, \dots, e_{i_t}$.

4. Construction of Tests for Dual Systems.

In the theory of relay-contact networks, sometimes, knowing a network Ω_1 , which realizes the function $f_1(x_1, x_2, \dots, x_n)$, it is possible to construct by a simple method a network Ω_2 , which realizes a certain function $f_2(x_1, x_2, \dots, x_n)$.

The question arises whether it is possible in some cases, knowing the test T_1 for the network Ω_1 , to find a test T_2 for a certain network Ω_2 and bypass laborious calculations.

To formulate the result let us give a series of definitions.

Definition. The function $f^* = \bar{f}(\bar{x}_1, \bar{x}_2, \dots, \bar{x}_n)$ is called dual to the function $f(x_1, x_2, \dots, x_n)$.

Definition. A network Ω is called *planar* if the network which is obtained from Ω by joining a source circuit between the poles can be homomorphically placed in a plane.

Definition. A network Ω^* is called dual with respect to the planar network Ω if it is constructed

in the following manner. The planar network \mathcal{Q} together with the source link breaks up the plane into regions. We choose in each plane one point -- the vertices of the future network. For the poles of \mathcal{Q}^* we take those vertices, which correspond to the regions that have the source circuit as part of the boundary. Next, each two vertices of "network \mathcal{Q}^* " is joined by means of contacts $\tilde{x}_{i1}, \tilde{x}_{i2}, \dots, \tilde{x}_{ip}$, where $\tilde{x}_{i1}, \tilde{x}_{i2}, \dots, \tilde{x}_{ip}$ are all the contacts located on the boundary between the corresponding regions; if both vertices are poles of \mathcal{Q}^* , we join them with the source circuit.

Example. Fig. 13 shows by means of solid lines the network \mathcal{Q} , and the dual network \mathcal{Q}^* is shown dotted.

From the definition it follows that \mathcal{Q}^* is a planar network.

As regards the dual networks, the following theorem is known, obtained by C. Shannon [7].

Theorem. If a function $f(x_1, x_2, \dots, x_n)$ is realized by a planar network \mathcal{Q} , then the dual network \mathcal{Q}^* realizes the dual function $f^*(x_1, x_2, \dots, x_n)$.

Proof. Let us run briefly through the proof of this theorem. Let the network \mathcal{Q}^* realize the function $f'(x_1, x_2, \dots, x_n)$. Let us consider the arbitrary assembly $\alpha_1, \alpha_2, \dots, \alpha_n$. Two cases are possible.

1) $f(\alpha_1, \alpha_2, \dots, \alpha_n) = 1$. This means that in the network \mathcal{N} there is a path that joins the poles a and b , and in the relay states $\alpha_1, \alpha_2, \dots, \alpha_n$ all the contacts along this path are closed. Corresponding to this path in the network \mathcal{N}^* is a set of contacts (of equal designation as the contacts of the path considered). With this, if all these contacts are open, and this takes place for the relay states $\bar{\alpha}_1, \bar{\alpha}_2, \dots, \bar{\alpha}_n$, then the network \mathcal{N}^* is open and, consequently, $f'(\bar{\alpha}_1, \bar{\alpha}_2, \dots, \bar{\alpha}_n) = 0$.

2) $f(\alpha_1, \alpha_2, \dots, \alpha_n) = 0$. In this case, for the state of the relays $\alpha_1, \alpha_2, \dots, \alpha_n$ the network is open. It follows therefore that there exists a path in the network \mathcal{N}^* , joining the poles a' and b' . With this, this path passes through the open contacts of the network \mathcal{N} . The latter means that at the relay states $\bar{\alpha}_1, \bar{\alpha}_2, \dots, \bar{\alpha}_n$ all the contacts on the constructed path are closed. We obtain

$$f'(\bar{\alpha}_1, \bar{\alpha}_2, \dots, \bar{\alpha}_n) = 1.$$

Thus, in both cases

$$f'(x_1, x_2, \dots, x_n) = f(x_1, x_2, \dots, x_n)$$

or

$$f'(x_1, x_2, \dots, x_n) = f(x_1, x_2, \dots, x_n) = f^*(x_1, x_2, \dots, x_n).$$

The theorem proved makes it possible to construct from a planar realization of the function $f(x_1, x_2, \dots,$

x_n) a network for the function $\tilde{f}(x_1, x_2, \dots, x_n)$.

Assume that a planar network \mathcal{O} realizes the function $f(x_1, x_2, \dots, x_n)$. We denote by M the set of faults of the network \mathcal{O} (closing or opening of contacts). We have seen that to each fault $a \in M$ there corresponds a fault function $f_a(x_1, x_2, \dots, x_n)$. The fault a breaks down the set of all the contacts of the network \mathcal{O} into three subsets: k_1 , k_2 , and k_3 , where k_1 consists of the contacts which are short circuited, k_2 of the open contacts, and k_3 of the remaining contacts. It is obvious that corresponding to this breakdown of the contacts of the network \mathcal{O} is a breakdown of the contacts of the network \mathcal{O}^* (the breakdown is generated by dual correspondence).

Let us consider the fault a^* (dual to the fault a) of the network \mathcal{O}^* , at which all the contacts of the set k_1 are open, the contacts of set k_2 are short circuited, and the remaining ones are in *proper* working order. We denote by M^* the set of faults a^* of the network \mathcal{O}^* , where a runs through the set M . From the preceding theorem it follows that the fault function $f_{a^*}(x_1, x_2, \dots, x_n)$ of the network \mathcal{O}^* , corresponding to the fault a^* , is

$$f_{a^*}(x_1, x_2, \dots, x_n) = [f_a(x_1, x_2, \dots, x_n)]^*.$$

It follows therefore that if $f_a(x_1, x_2, \dots, x_n)$ is the fault function of the network \mathcal{N} , then the fault function $f_{a^*}^*(x_1, x_2, \dots, x_n)$ for the fault a^* of the network \mathcal{N}^* is dual to $f_a(x_1, x_2, \dots, x_n)$.

Let \mathcal{M} be the set of different fault functions of the network \mathcal{N} corresponding to the faults M . Then, denoting by \mathcal{M}^* the set of fault functions of the network \mathcal{N}^* corresponding to the faults M^* . Let \mathcal{N} be a certain subset of unordered pairs of functions (f_a, f_b) of the set \mathcal{M} , excluding the pairs (f_a, f_b) where $f_a \equiv f_b$. We place this subset in correspondence with the subset \mathcal{M}^* of the pairs $(f_{a^*}^*, f_{b^*}^*)$ of the set \mathcal{M}^* . Obviously, \mathcal{N}^* does not contain pairs of the form $(f_{a^*}^*, f_{b^*}^*)$ where $f_{a^*}^* \equiv f_{b^*}^*$, since we would have from the foregoing result $(f_a)^* = (f_b)^*$ or $f_a \equiv f_b$, which contradicts the definition of the set \mathcal{N} .

Theorem. Let $T = \{(\alpha_1, \alpha_2, \dots, \alpha_n)\}$ be a test relative to the subset \mathcal{N} for the network \mathcal{N} and then $T^* = \{(\bar{\alpha}_1, \bar{\alpha}_2, \dots, \bar{\alpha}_n)\}$ is a test relative to the subset \mathcal{M}^* for the network \mathcal{N}^* , and vice versa.

Proof. In fact, let $(f_a(x_1, x_2, \dots, x_n), f_b(x_1, x_2, \dots, x_n)) \in \mathcal{N}$. Since T is a test, there exists an assembly $(\alpha_1, \alpha_2, \dots, \alpha_n) \in T$ such that

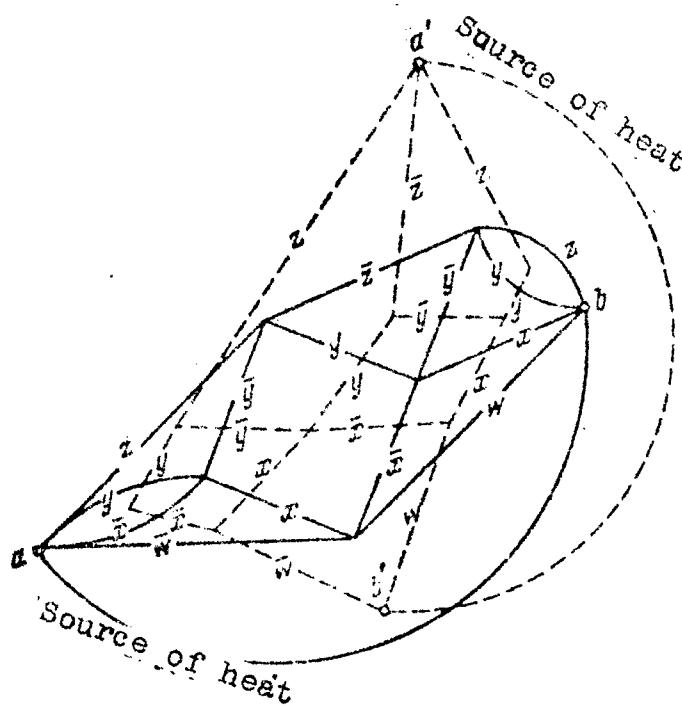


Fig. 13

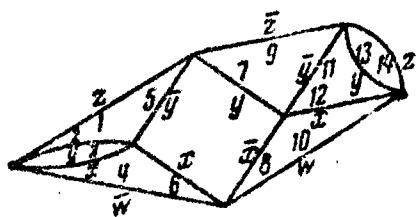


Fig. 14

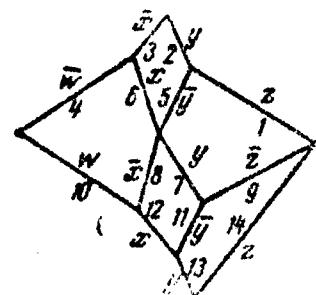
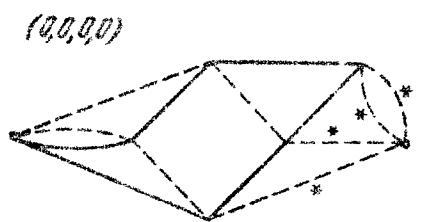
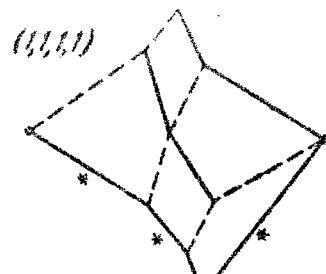


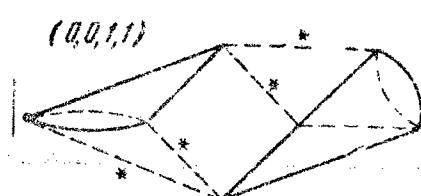
Fig. 15



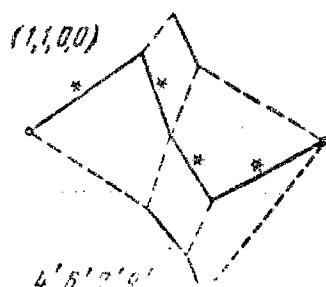
$10, 12, 13, 14$



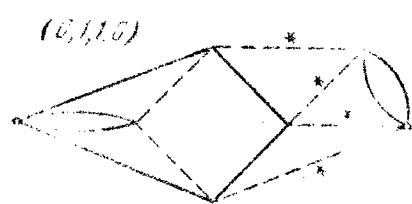
$10', 12', 13', 14'$



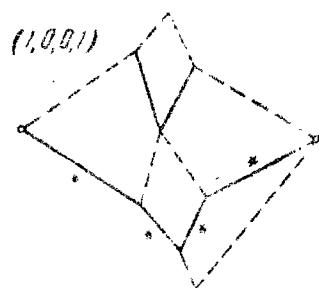
$4, 5, 7, 9$



$4', 5', 7', 9'$



$4, 10, 11, 12$



$3', 2', 11', 12'$

Fig. 16a

Fig. 17a

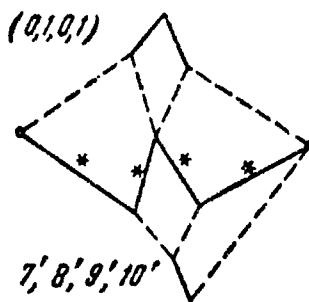
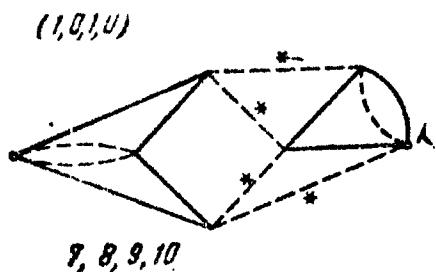
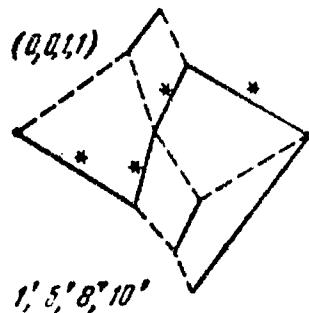
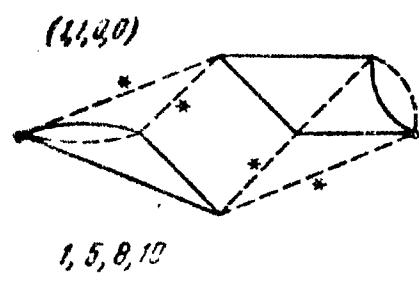
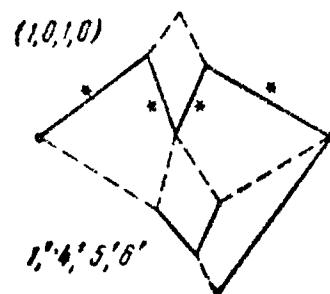
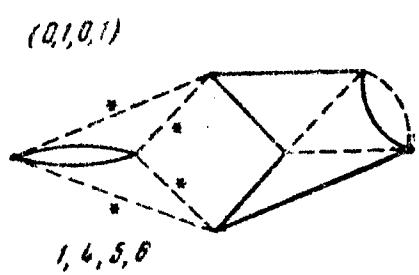
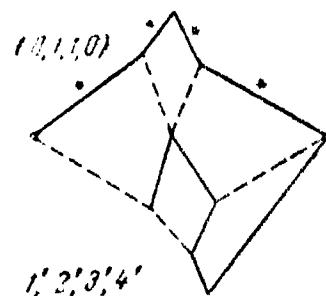
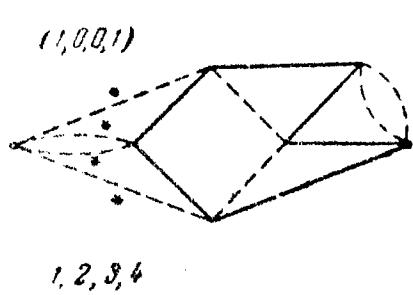


Fig. 16b

Fig. 17b

$$f_a(a_1, a_2, \dots, a_n) \neq f_b(a_1, a_2, \dots, a_n).$$

From this we obtain

$$f_a(\bar{a}_1, \bar{a}_2, \dots, \bar{a}_n) \neq f_b(\bar{a}_1, \bar{a}_2, \dots, \bar{a}_n)$$

or

$$[f_a(a_1, a_2, \dots, a_n)]^* \neq [f_b(a_1, a_2, \dots, a_n)]^*.$$

Taking into consideration the connection between the fault functions of the network \mathcal{N} with the fault functions of the network \mathcal{N}^* , we obtain

$$f_{a^*}(a_1, a_2, \dots, a_n) \neq f_{b^*}(a_1, a_2, \dots, a_n).$$

Consequently, T^* is a test relative to \mathcal{N}^* for the network \mathcal{N}^* .

The inverse statement follows from the following relations:

$$g^{**} = g, \quad \mathfrak{M}^{**} = \mathfrak{M}, \quad \mathfrak{N}^{**} = \mathfrak{N}, \quad T^{**} = T.$$

Corollary. Corresponding to the minimal test with respect to \mathcal{N} of the network \mathcal{N} is a minimal test with respect to \mathcal{N}^* of the network \mathcal{N}^* .

Example. For the sake of illustrating the proved theorem, let us give an example in which we construct in parallel a test for a planar network \mathcal{N} and a dual network \mathcal{N}^* , in the case when the permissible fault is the closing or opening of some single contact. Attention should be called here that the closing of $\underset{\wedge}{a}$ contact in network \mathcal{N} corresponds to

opening of contact α in network \mathcal{N}^* and vice versa. As in the preceding examples, cases of closing and opening of the contacts are independent, and are therefore analyzed separately.

Network \mathcal{N} (Fig. 14) realizes the function

$$\begin{aligned} S_{1,3,4}(x, y, z, w) = & x\bar{y}z w \vee x\bar{y}z\bar{w} \vee \\ & \vee x\bar{y}z\bar{w} \vee x\bar{y}z w \vee x\bar{y}z\bar{w} \vee x\bar{y}z w \vee \\ & \vee x\bar{y}z w \vee x\bar{y}z\bar{w} \vee x\bar{y}z w \end{aligned}$$

while network \mathcal{N}^* (Fig. 15), which is dual to network \mathcal{N} , realizes the function

$$\begin{aligned} S_{2,4}(x, y, z, w) = & x\bar{y}z w \vee x\bar{y}z\bar{w} \vee \\ & \vee x\bar{y}z\bar{w} \vee x\bar{y}z w \vee x\bar{y}z\bar{w} \vee x\bar{y}z\bar{w} \vee x\bar{y}z w \end{aligned}$$

The fault functions in the case of closing (network \mathcal{N}) are shown in Fig. 16, while the fault functions for the case of opening (network \mathcal{N}^*) are shown in Fig. 17.

By gathering together the states of the networks for different values of the assemblies shown in Fig. 16, we obtain a table for the fault functions for closing (Table 3). Similarly, by gathering the states of the networks for different values of the assemblies shown in Fig. 17, we obtain a table of fault functions for opening (see Table 4).

Table 3

(x, y, z, w)	0	1	2	3	4	5	6	7	8	9	10	11	12	13	14
$(0, 0, 0, 0)$	0									1			1	1	1
$(0, 0, 1, 1)$	0				1		1	1		1					
$(0, 1, 0, 1)$	0	1			1	1	1								
$(0, 1, 1, 0)$	0									1	1	1	1		
$(1, 0, 0, 1)$	0	1	1	1	1										
$(1, 0, 1, 0)$	0							1	1	1	1				
$(1, 1, 0, 0)$	0	1				1			1		1				

 $f_2 = f_3$ $f_{13} = f_{14}$

Table 4

(x, y, z, w)	0	1'	2'	3'	4'	5'	6'	7'	8'	9'	10'	11'	12'	13'	14'
$(1, 1, 1, 1)$	1										0		0	0	0
$(1, 1, 0, 0)$	1				0	0	0	0							
$(1, 0, 1, 0)$	1	0			0	0	0								
$(1, 0, 0, 1)$	1									0	0	0	0		
$(0, 1, 1, 0)$	1	0	0	6	0										
$(0, 1, 0, 1)$	1								0	0	0	0			
$(0, 0, 1, 1)$	1	0				0			0		0				

$$f_2 = f_3, \quad f_{13} = f_{14}$$

Let us
construct expression $\Pi\Sigma$

$$0 \left\{ \begin{array}{l} 10, 12, 13 \\ 0, 1, 2, 4, 5, 6, 7, 8, 9, 11 \end{array} \right.$$

$$6 \left\{ \begin{array}{l} 10, 12 \\ 3 \end{array} \right. \left\{ \begin{array}{l} 9, 11 \\ 0, 1, 2, 4, 5, 6, 7, 8 \end{array} \right.$$

$$9 \left\{ \begin{array}{l} 1, 2, 4 \\ 0, 5, 6, 7, 8 \end{array} \right.$$

Let us
construct expression $\Pi\Sigma$

$$15 \left\{ \begin{array}{l} 10', 12', 13' \\ 0, 1', 2', 4', 5', 6', 7', 8', 9', 11' \end{array} \right.$$

$$9 \left\{ \begin{array}{l} 10', 12' \\ 13' \end{array} \right. \left\{ \begin{array}{l} 9', 11' \\ 0, 1', 2', 4', 5', 6', 7', 8' \end{array} \right.$$

$$6 \left\{ \begin{array}{l} 1', 2', 4' \\ 0, 5', 6', 7', 8' \end{array} \right.$$

$10 \cdot 12$	$10 \vee 12$	$0 \cdot 7$	$3 \vee 10$	$10' \cdot 12'$	$3 \vee 5$	$0 \cdot 7'$	$5 \vee 12$
$9 \cdot 11$	$3 \vee 10$	$0 \cdot 8$	$10 \vee 12$	$9' \cdot 11'$	$5 \vee 12$	$0 \cdot 8'$	$3 \vee 5$
$1 \cdot 2$	$5 \vee 12$	$5 \cdot 6$	$3 \vee 12$	$1' \cdot 2'$	$3 \vee 10$	$5' \cdot 6'$	$3 \vee 12$
$1 \cdot 4$	$3 \vee 12$	$5 \cdot 7$	$3 \vee 5 \vee 10 \vee 12$	$1' \cdot 4'$	$3 \vee 12$	$5' \cdot 7'$	$3 \vee 5 \vee 10 \vee 12$
$2 \cdot 4$	$3 \vee 5$	$5 \cdot 8$	$5 \vee 10$	$2' \cdot 4'$	$10 \vee 12$	$5' \cdot 8'$	$5 \vee 10$
$0 \cdot 5$	$5 \vee 12$	$6 \cdot 7$	$5 \vee 10$	$0 \cdot 5'$	$3 \vee 10$	$6' \cdot 7'$	$5 \vee 10$
$0 \cdot 6$	$3 \vee 5$	$6 \cdot 8$	$3 \vee 5 \vee 10 \vee 12$	$0 \cdot 6'$	$10 \vee 12$	$6' \cdot 8'$	$3 \vee 5 \vee 10 \vee 12$
		$7 \cdot 8$	$3 \vee 12$			$7' \cdot 8'$	$3 \vee 12$

$$\Pi\Sigma = 0 \cdot 6 \cdot 9 (10 \vee 12) (3 \vee 10) (5 \vee 12) (5 \vee 10) (3 \vee 5) (3 \vee 12) (10 \vee 12)$$

$$(3 \vee 12) (10 \vee 12) (5 \vee 10)$$

The expressions for $\Pi\Sigma$ go into each other when the assemblies are replaced by their duals. It follows therefore that ~~each~~^{to} test of one expression there corresponds a test of the other expression, and vice versa.

For the case of opening, the fault functions are shown in Fig. 18, and for the case of closing, the fault functions are shown in Fig. 19.

Gathering together the states of the networks for different values of the assemblies shown in Fig. 18, we obtain the fault functions for the constructed functions (Table 5). Similarly, gathering together the states of the networks for different values of the assemblies shown in Fig. 19, we obtain Table 6 for the fault functions.

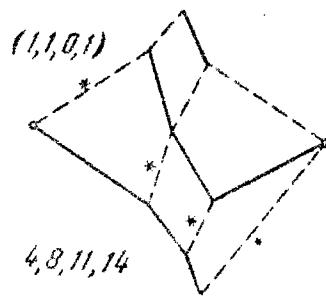
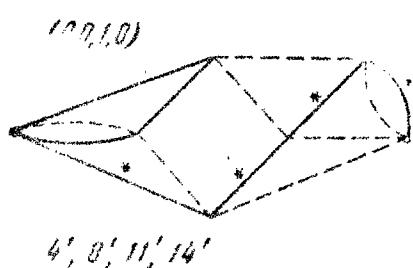
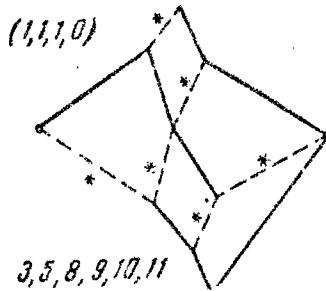
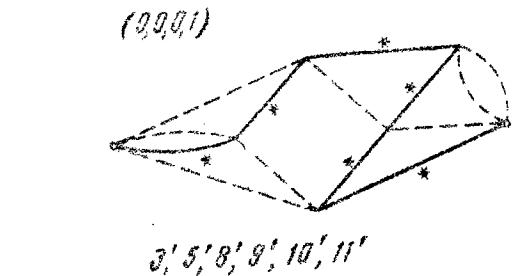


Fig. 18

Fig. 19

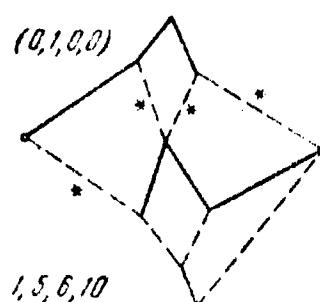
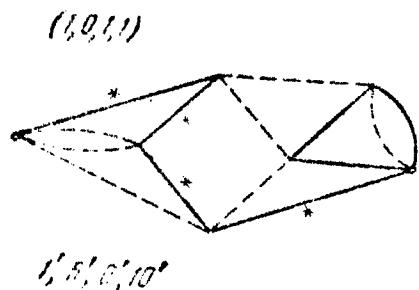
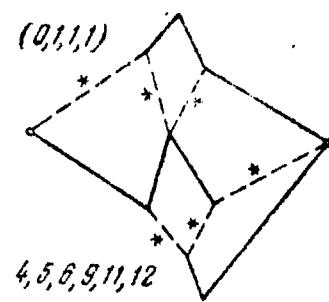
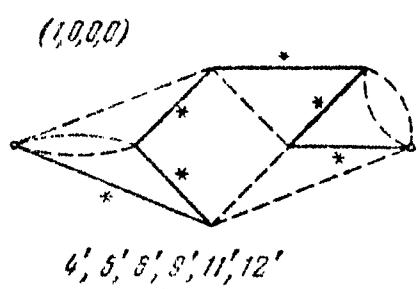
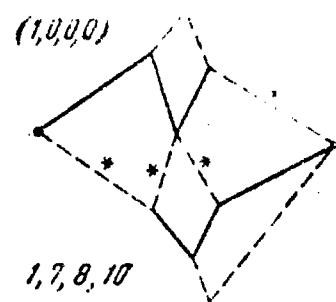
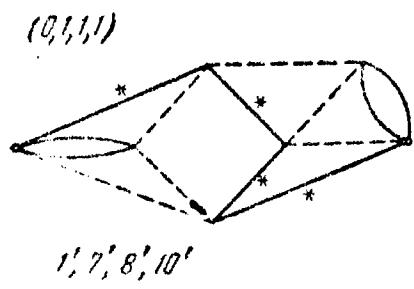
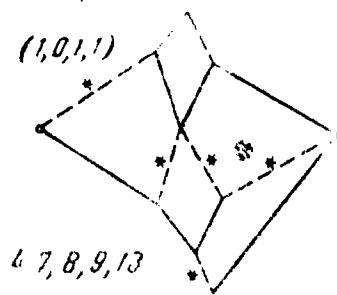
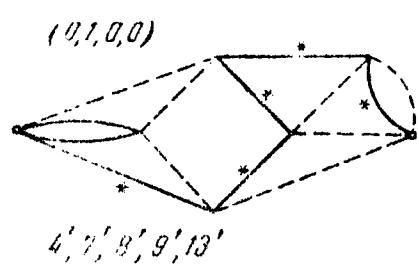


Fig. 18"

Fig. 19"

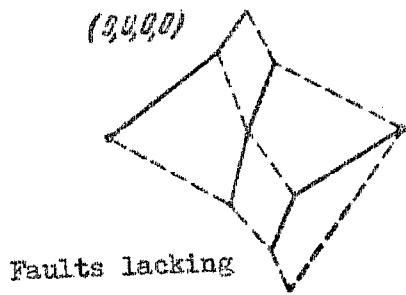
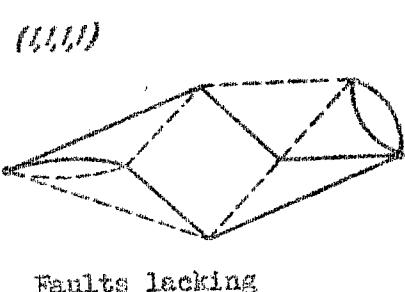
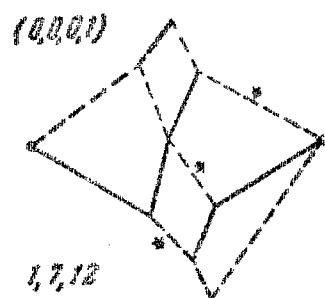
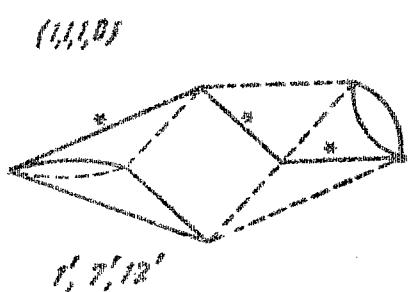
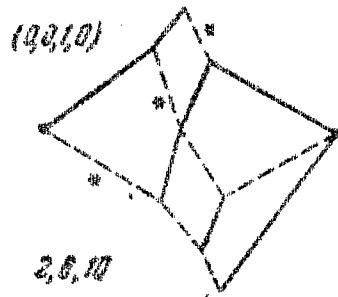
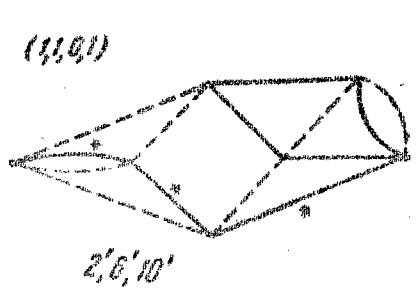


Fig. 18'''

Fig. 19'''

Table 5

(x, y, z, w)	0	1	2	3	4	5	6	7	8	9	10	11	12	13	14
$(1, 1, 1, 1)$	1														
$(1, 1, 1, 0)$	1	0													
$(1, 1, 0, 1)$	1	0	0												
$(1, 1, 0, 0)$	1	0	0	0											
$(1, 0, 1, 1)$	1	0	0	0	0										
$(1, 0, 1, 0)$	1	0	0	0	0	0									
$(1, 0, 0, 1)$	1	0	0	0	0	0	0								
$(1, 0, 0, 0)$	1	0	0	0	0	0	0	0							
$(0, 1, 1, 1)$	0	1	1	0											
$(0, 1, 1, 0)$	0	1	1	0	0										
$(0, 1, 0, 1)$	0	1	0	1	0										
$(0, 1, 0, 0)$	0	1	0	0	1	0									
$(0, 0, 1, 1)$	0	0	1	1	0	0									
$(0, 0, 1, 0)$	0	0	1	0	1	0									
$(0, 0, 0, 1)$	0	0	0	1	1	0									
$(0, 0, 0, 0)$	0	0	0	0	0	1	1	0	0	0	0	0	0	0	0

Table 6

(x, y, z, w)	0	1	2	3	4	5	6	7	8	9	10	11	12	13	14
$(1, 1, 1, 0)$	0	1	1	1	1	1	1	1	1	1	1	1	1	1	1
$(1, 1, 0, 1)$	0	1	1	1	1	1	1	1	1	1	1	1	1	1	1
$(1, 0, 1, 1)$	0	1	1	1	1	1	1	1	1	1	1	1	1	1	1
$(1, 0, 0, 0)$	0	1	1	1	1	1	1	1	1	1	1	1	1	1	1
$(0, 1, 1, 1)$	0	1	1	1	1	1	1	1	1	1	1	1	1	1	1
$(0, 1, 0, 0)$	0	1	1	1	1	1	1	1	1	1	1	1	1	1	1
$(0, 0, 1, 0)$	0	1	1	1	1	1	1	1	1	1	1	1	1	1	1
$(0, 0, 0, 1)$	0	1	1	1	1	1	1	1	1	1	1	1	1	1	1
$(0, 0, 0, 0)$	0	1	1	1	1	1	1	1	1	1	1	1	1	1	1

Let us con-
struct expression $\Pi\Sigma$

$$\begin{cases} 3', 5', 8', 9', 10', 11' \\ 0, 1', 2', 4', 6', 7', 12', 13', 14' \end{cases}$$

$$\begin{cases} 4', 14' \\ 0, 1', 2', 6', 7', 12', 13' \end{cases} \begin{cases} 8', 11' \\ 3', 5', 9', 10' \end{cases}$$

$$\begin{cases} 4' \\ 14' \end{cases} \begin{cases} 6' \\ 11' \end{cases} \begin{cases} 7', 13' \\ 0, 1', 2', 6', 12' \end{cases} \begin{cases} 9' \\ 3', 5', 10' \end{cases}$$

$$\begin{cases} 2', 6' \\ 0, 1', 12' \end{cases} \begin{cases} 10' \\ 3', 5' \end{cases}$$

$$\begin{array}{l|l} 2' \cdot 6' & 8 \vee 11 \\ 0 \cdot 1' & 7 \vee 11 \vee 14 \\ 0 \cdot 12' & 8 \vee 14 \\ 1' \cdot 12' & 7 \vee 8 \vee 11 \\ 3' \cdot 5' & 8 \vee 11 \\ 7' \cdot 13' & 7 \vee 14 \end{array}$$

Let us con-
struct expression $\Pi\Sigma$

$$\begin{cases} 3, 5, 8, 9, 10, 11 \\ 0, 1, 2, 4, 6, 7, 12, 13, 14 \end{cases}$$

$$\begin{cases} 4, 14 \\ 0, 1, 2, 6, 7, 12, 13 \end{cases} \begin{cases} 8, 11 \\ 3, 5, 9, 10 \end{cases}$$

$$\begin{cases} 4 \\ 14 \end{cases} \begin{cases} 8 \\ 11 \end{cases} \begin{cases} 7, 13 \\ 0, 1, 2, 6, 12 \end{cases} \begin{cases} 9 \\ 3, 5, 10 \end{cases}$$

$$\begin{cases} 2, 6 \\ 0, 1, 12 \end{cases} \begin{cases} 10 \\ 3, 5 \end{cases}$$

$$\begin{array}{l|l} 2 \cdot 6 & 4 \vee 7 \\ 0 \cdot 1 & 1 \vee 4 \vee 8 \\ 0 \cdot 12 & 1 \vee 7 \\ 1 \cdot 12 & 4 \vee 7 \vee 8 \\ 3 \cdot 5 & 4 \vee 7 \\ 7 \cdot 13 & 1 \vee 8 \end{array}$$

As in the preceding case, we verify that to each test of one expression there corresponds a test of the other expression, and vice versa.

5. Single Tests

As follows from the definition, the form of a test for verifying one and the same network \mathcal{Q} , realizing a function $f(x_1, x_2, \dots, x_n)$, depends on the choice of the set \mathcal{N} . In other words, the form of the test depends on the fixation of the permissible faults, and also on the degree of detail to which it is necessary to carry out the analysis of the faults.

From this point of view, it is possible to classify the tests. We shall not dwell in detail on this question. We shall note, however, a few types of tests.

1. A single test for the detection of a faulty contact, when it is known beforehand that the fault (closing or opening of the contact) is possible for any contact, but also for one.

2. Test of a relay for detecting faulty relays --- the permissible faults are a short circuit or an open circuit in the device that controls the connection of the power supply to the relay winding. In this case, as can be readily seen, the form of the

test depends only on the function and is independent of the choice of the network that realizes the given function.

3. Complete test for the detection of faults in contacts, when the permissible faults are a shorting or an opening of any contact (possibly of several contacts simultaneously). It is obvious that any test for a contact network is contained in a certain complete test.

It is important to note here that although the form of the test depends on the choice of the set \mathcal{N} , which in the final analysis depends on the structure of the network, in many cases one can start ^{out} not from a specification of the set \mathcal{N} , but from a list of certain requirements which are independent of the form of the network. This, for example, is the situation for the foregoing types of tests. In those cases when the problem is formulated in terms which do not take into account the structure of the network, it becomes meaningful to raise the question of comparing tests corresponding to different networks.

Let $t_{f(x_1, x_2, \dots, x_n)}$ be the shortest length of the test in the examination of all the network realizations of a function $f(x_1, x_2, \dots, x_n)$. Let furthermore

$$t(n) = \max_f t_{f(x_1, x_2, \dots, x_n)},$$

where max is taken over all the functions of algebraic logic, which depend on n arguments. Then, naturally, the following problem arises.

What is the asymptotic expression for the function $t(n)$ for any type of test? It is clear here that $t(n) \leq 2^n$.

For example, it is unknown whether $t(n) < 2^n$ in the case of complete tests. In other words, how sensible is the formulation of the problem concerning a minimal test (see note in connection with the definition of the complete test).

Along with these questions, one must also raise several other questions concerning tests.

1) How are tests changed when networks are transformed?

2) Let \mathcal{M} be the set of different fault functions of the network \mathcal{N} for a given type of test. What is the estimate of the cardinality of the set \mathcal{M} ? (in this way we can obtain an estimate for $t(n)$).

Let us proceed now to a more detailed examination of unit tests. We are concerned with unit tests because this case is in some sense the simplest. Whereas, for example, in the case of a complete test, even for simple

networks with 5 or 6 contacts, large calculations are necessary to construct the tables of fault functions (if ℓ is the number of network contacts, 3^ℓ faults are possible).

Since for any $\varepsilon > 0$ one can indicate such a N , that any function of $n > N$ arguments can be realized with a network with a number of contacts not greater than $(1 + \varepsilon) 2^{n+2}/n$ [8], then for $n \geq N$

$$t(n) \leq (1 + \varepsilon) \frac{2^{n+3}}{n}.$$

The latter follows from the fact that the length of the test does not exceed the number of all the fault functions.

It follows from this result that when

$$(1 + \varepsilon) \frac{2^{n+3}}{n} \leq 2^n, \text{ i. e. } n \geq 8(1 + \varepsilon)$$

the problem of finding the minimal test has a full meaning in that the length of the minimal test, roughly speaking, amounts to $8/n$ of 2^n --- the length of the trivial test.

We have seen in Sec. 3 that a unit test breaks up into two independent (non-intersecting) tests: a test for a short and a test for an open circuit. Consequently, the problem of the construction of a single test breaks down into two independent problems.

For further analysis it is useful to investigate

the tests from the geometrical point of view.

Let $f(x_1, x_2, \dots, x_n)$ be realized by the network

Q. To each function $f(x_1, x_2, \dots, x_n)$ one can set in relative unique correspondence a certain subset P of vertices of a unit n-dimensional cube; precisely,

P is a set of all such points $\alpha = \{\alpha_1, \alpha_2, \dots, \alpha_n\}$ that

$$f(x_1, x_2, \dots, x_n) = 1.$$

For example (Fig. 20)

$$f(x_1, x_2, x_3) = x_1 + x_2 + x_3 \pmod{2},$$

$$P = \{(1, 0, 0), (0, 1, 0), (0, 0, 1), (1, 1, 1)\}.$$

Let us put

$$\mathcal{M} = \mathcal{M}_q + \mathcal{M}_r,$$

where \mathcal{M}_q is the set of fault functions in the case of a single closing, \mathcal{M}_r the set of fault functions in the case of a single opening. We denote by Q the set of "closings", i.e., the set of all those vertices of the n-dimensional cube, in each of which all the functions from \mathcal{M}_q do not assume one and the same value. Analogously, R is the set of points of "openings," i.e., the set of all those vertices of the n-dimensional cube, in each of which all the functions from \mathcal{M}_r do not assume one and the same value.

Obviously we have

$$Q \subset C P \text{ (complement to } P), R \subset P.$$

We introduce on the set of the vertices of the unit n -dimensional cube the following metric (see [4])

$$\rho(\alpha, \beta) = |\alpha_1 - \beta_1| + |\alpha_2 - \beta_2| + \dots + |\alpha_n - \beta_n|.$$

Let M be a certain subset of the points of the vertices of the unit n -dimensional cube. We denote by $S(M, 1)$ the set of points p of the unit n -dimensional cube, such that there is found a point $m \in M$, for which $\rho(p, m) = 1$.

We consider the set $P \setminus S(P, 1)$. Those sets assemblies from Q , which enter into this set, are called false. False assemblies are due to the presence of false circuits in the network (compare with Sec. 1).

We note that the set Q can coincide with CP and R can coincide with P . For this purpose it is necessary to realize $f(x_1, x_2, \dots, x_n)$ by means of a $\overline{\Pi}$ network, corresponding to the conjunctive normal form and respectively to the disjunctive normal form.

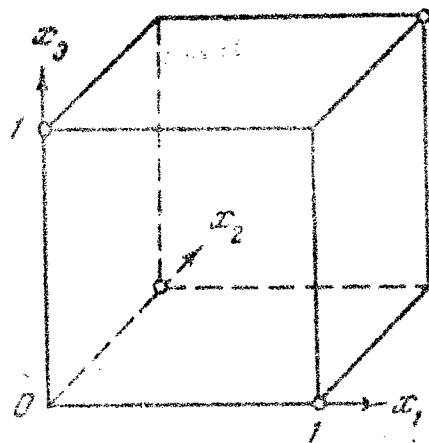


Fig. 20

	\bar{x}_1	\bar{x}_2	\bar{x}_3	\bar{x}_{K-1}	\bar{x}_K	\bar{x}_{K+1}	\bar{x}_{K+2}
1	\bar{x}_1 x_2	\bar{x}_2 x_3	\bar{x}_3		\bar{x}_{K-1} x_K	\bar{x}_K x_{K+1}	\bar{x}_{K+1}
2	\bar{x}_2 x_3	\bar{x}_3 x_4	\bar{x}_4		\bar{x}_K	\bar{x}_{K+1}	\bar{x}_{K+2}
$n-K-1$	\bar{x}_{n-K}	\bar{x}_{n-K+1}			\bar{x}_{n-2}	\bar{x}_{n-1}	
$n-K$	\bar{x}_{n-K}	\bar{x}_{n-K+1}	\bar{x}_{n-K+2}		\bar{x}_{n-2}	\bar{x}_{n-1}	\bar{x}_n
	x_{n-K+1}	x_{n-K+2}			x_{n-1}	x_n	

Fig. 21

Chapter II

Methods of Constructing Tests for Individual Classes of Networks

The investigations of Chapter I show that the general algorithm is too cumbersome even in the case of construction of minimal single tests. Apparently, the cumbersomeness of this algorithm is due to its universality (i.e., due to the circumstance that it is suitable for any function $f(x_1, x_2, \dots, x_n) \in P_2$ and any network \mathcal{U} that realizes it). One could dispense with the requirement of minimality, replacing it with the requirement that the length of the test, for the network \mathcal{U} , realizing the function $f(x_1, x_2, \dots, x_n)$ have an order not exceeding the order $t(n)$, i.e., the order of the greatest length of all the lengths of the minimal tests over all the functions of n arguments. We shall not touch upon this question. One can advance here the assumption that the general algorithms, as in the case of the synthesis of relay-contact networks, will give, for individual networks (although they are simpler than the common algorithm for the construction of the minimal test), greater deviations from the minimal test. Taking these considerations into account, one can indicate two paths in test theory: on the one

hand, one can forgo an examination of all the functions and all the networks, and on the other hand one can modify the concept of a test, for example require that the error occur with a probability, say, greater than $1 - \epsilon$.

In the present chapter we shall touch upon the first side of the matter. Here the problem of construction of tests is solved for individual classes of functions with allowance for the singularities of the synthesis of the networks. In these considerations, a decisive role is played not by the table of functions, but by the method of specifying the table, ^{one which} takes into account certain contentful singularities of the structure of the functions.

6. Tests for Networks that Realize Elementary Symmetrical Functions

In the study of symmetrical functions from P_2 , a fundamental role is played by the so called elementary symmetrical functions, i.e., functions of the form

$$S_k(x_1, x_2, \dots, x_n) = \bigvee x_1^{a_1} \& x_2^{a_2} \& \dots \& x_n^{a_n},$$

$$a_1 + a_2 + \dots + a_n = k,$$

$$\text{where } x^a = \begin{cases} x & \text{for } a = 0, \\ x & \text{for } a = 1. \end{cases}$$

The function S_k assumes a value of 1 for those and only those assemblies $(\alpha_1, \alpha_2, \dots, \alpha_n)$ in which 1 is encountered exactly k times.

As is known //7/, the function $S_k(x_1, x_2, \dots, x_n)$ can be realized by a network $\gamma_{n,k}$ with $k(n - k + 1) + (n - k)(k + 1)$ contacts (Fig. 21). For this class of networks, the question arises of the construction of a sufficiently "good" single test for closing. This problem is of interest in connection with the fact that the construction of a single test reduces to the construction of a single test for closing and a single test for opening. For this purpose, we establish the following proposition.

Theorem. For the network $\gamma_{n,k}$, $\text{rank}(k, n - k) \geq 2$, one can construct a single short-circuit ^{circuit} test Γ of length t ,

where

$$t \leq (n - k + 1)(k - 2) + (n - k) + \left[\frac{n - k + 1}{2} \right] + 2 \text{ npu } k \geq 3,$$

$$t \leq (k + 1)(n - k - 2) + k + \left[\frac{k + 1}{2} \right] + 2 \text{ npu } n - k \geq 3,$$

$$\left. \begin{array}{l} t = 7 \text{ npu } n = 4, k = 2 \\ t = 4 \text{ npu } n = 3, k = 1, 2 \end{array} \right\} \max(k, n - k) = 2.$$

For convenience, we renumber the contacts of the network $\gamma_{n,k}$ in the following manner: we introduce a system of coordinates, as indicated in Fig. 21, and set

in correspondence each "horizontal" (closing) contact the coordinates $(i, j)_h$ of its left end (the first coordinate is reckoned along the horizontal axis, the second along the vertical one), and to each "vertical" (opening) contact we set in correspondence the coordinates $(i, j)_v$ of its upper end. Obviously, for the coordinates $(i, j)_h$ we have $0 \leq i \leq k-1$ and $0 \leq j \leq n-k$; for the coordinates $(i, j)_v$ we have $0 \leq i \leq k$ and $0 \leq j \leq n-k-1$.

We shall construct a test in the form $T = T_1 + T_2 + T_3 + T_4$. Simultaneously we shall verify that with the aid of T one can establish any single closing in the network $\gamma_{n,k}$ and thereby prove that T is a test. We put $k \geq 2$.

1) With the aid of the assemblies T_1 we determine that: a) either a vertical contact is out of order, b) or else a horizontal contact is out of order or the circuit is in working order.

Let the aggregate T_1 of the assemblies be defined in the following manner:

		$n-k-1$		$k+1$					
$n-k$	0	0	...	0	1	1	...	1	1
	0	0	...	1	1	1	...	1	0
	0	1	...		1	1	0	...	0
	1	1	...	1	0	0	...	0	

On the assembly

$$\overbrace{0 \dots 0}^{l-1} \overbrace{1 \dots 1}^{k+1} 0 \dots 0$$

the correct network $\gamma_{n,k}$ assumes the form shown in Fig. 22.

Consequently, the network operates if and only if a single closing is contained in the vertical contacts of the l -th horizontal strip. If for all the assemblies T_1 the network does not conduct, then either the network is in working order or else there is a single fault in the horizontal contacts. We note that here in the case of a fault in the vertical contacts, we establish even the strip in which the faulty contact is located.

2) Let us assume that either a horizontal contact is faulty, or else the circuit is in working order. We shall show how to continue the analysis of the circuit in this case. Let us consider the set T_2 , consisting of two assemblies

$$\begin{aligned} \alpha) \quad & \overbrace{0 \dots 0}^{s-k+1} 1 \dots 1 \\ \beta) \quad & 1 \dots 1 \overbrace{0 \dots 0}^{s-k+1} \end{aligned}$$

Obviously, on these assemblies the network $\gamma_{n,k}$ assumes correspondingly the forms shown in Fig. 23. It is clear that in the case of assembly α the network conducts if and only if the horizontal contact of the 1-st column is

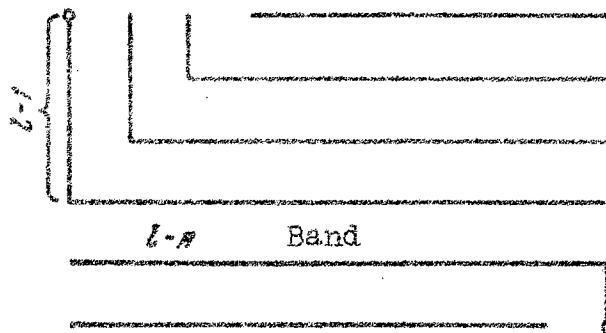


Fig. 22

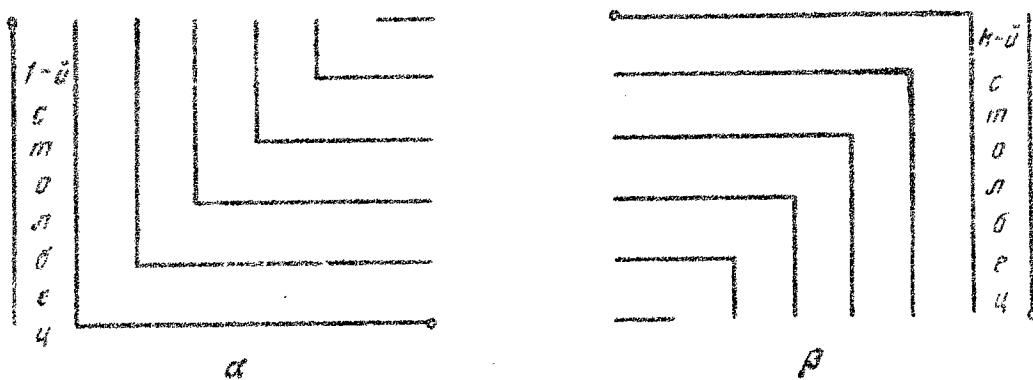


Fig. 23

faulty. In the case of assembly β_j it conducts when a horizontal contact of the last (k -th) column is at fault. If with both assemblies the circuit does not conduct, we have a third possibility: either the network is in working order, or else the horizontal contact in the "middle" columns is faulty. (When $k = 2$, in this case, the circuit is in working order).

a) Let us assume now that either the network is in working order, or else a horizontal contact in a middle column ($k > 2$) is faulty. In this case we consider the set \mathcal{B}_3 of assemblies

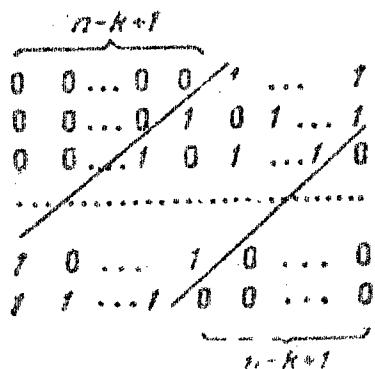
		$n-k$		$k-2$	
$k-2$		0	...	001011	...
		0	...	001101	...
	
		0	...	001111	...
		$n-k-1$			
$n-k+1$	$k-2$	0	...	010111	...
		0	...	011011	...
	
		0	...	011111	...
		\vdots			
$k-2$		101	...	110	...
		110	...	110	...
	
		111	...	010	...

We take the i -th assembly in the j -th box

$$\underbrace{0 \dots 0}_{n-k-j+1} \underbrace{1 \dots 1}_i \underbrace{0 \dots 0}_{k-i-1} \dots 0.$$

With this assembly, the network assumes the form shown in Fig. 24. Consequently, under the assumptions made ($k - 2 \geq i \geq 1$) the network operates if and only if the horizontal contact $(i, n - k - j + 1)_h$ is faulty. In the case when the network does not conduct on the assemblies from T_3 , it is in working order.

b) A horizontal contact of the first (or respectively last) column is faulty. Let us consider the aggregate of assemblies for $k \geq 3$.



This aggregate consists of the assemblies of the set T_2 and the first assemblies of each box of the set T_3 . If $k = 2$, then we add to the set T_2 , for $n = 3$, the assembly $\{0, 1, 0\} = T_3$, for $n = 4$ we add the assemblies $\{0, 0, 1, 0$ and $0, 1, 0, 0\} = T_3$. Let $k \geq 3$. Then with the $(j + 1)$ -th assembly ($1 \leq j \leq n - k + 1$) the network has the form shown in Fig. 25.

Let us write out the table of fault functions corresponding to respectively to the contacts $(0, 0)_h$, $(0, 1)_h$, ..., $(0, n - k)_h$, $(k - 1, 0)_h$, $(k - 1, 1)_h$, ...,

$(k-1, n-k)_h$ with the indicated assemblies (Table 7). It is seen from Table 7 that with the considered assemblies the faults in the horizontal contacts of the first and last columns is completely localized. In the case $k = 2$ it is easy to verify that it is also established which horizontal contact is faulty (under the condition that a horizontal contact is faulty).

3) Assume now that it is known that one of the vertical contacts of the l -th strip is faulty.

a) We put first $k \geq 3$. With the assemblies contained in $(n-k-l)$ -th box ($0 \leq l \leq n-k-1$), and the last assembly contained in the $(n-k-l+1)$ -th box, we make up a table of fault functions (Table 8), corresponding to the contacts

$(1, l)_v, (2, l)_v, \dots, (k-1, l)_v$. It is clear therefore that when $k \geq 3$ the fault in the contacts $(1, l)_v, (2, l)_v, \dots, (k-1, l)_v$ (i.e., vertical contacts of the $(l+1)$ -th strip excluding the extreme contacts) is established. In the case $k = 2$ for $n = 3$ we take the assembly $(0, 1, 0)$ and the assemblies $(0, 0, 1, 0)$ and $(0, 1, 0, 0)$ for the case $n = 4$ (see 2,

item "b"). With the aid of these assemblies presence of we detect the faults in all the vertical contacts, with the exception of contacts $(0, i)_v$ and $(k, i)_v$. If with the indicated assemblies the network does not conduct,

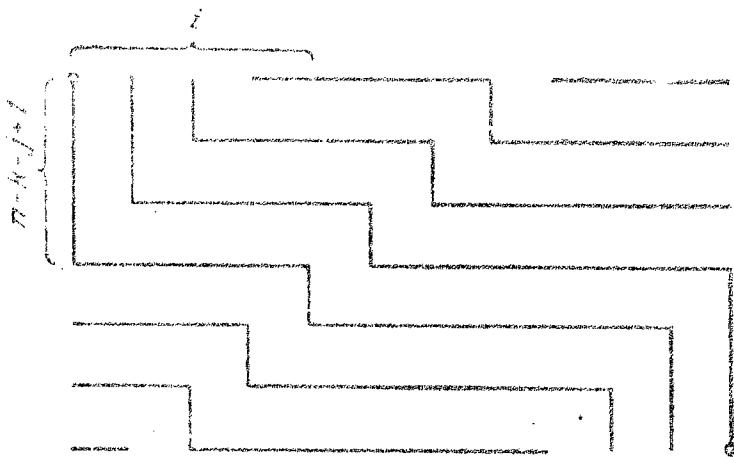


Fig. 24

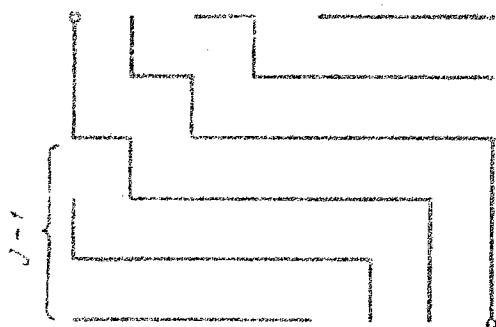


Fig. 25

we have case "b," i.e., the vertical contacts of the form $(0, i)_v$ and $(k, i)_v$ are faulty.

Table 7

	$(G_1)_v$	$(G_2)_v$...	$(G_{k-1})_v$	$(G_k)_v$	$(G_{k+1})_v$	$(G_{k+2})_v$...	$(G_{n-1})_v$	$(G_n)_v$
0 0 ... 0 0 / 1 ... 1	1	1	...	1	1	0	0	...	0	0
0 0 ... 0 1 0 1 ... 1	1	1	...	1	0	0	0	...	0	0
0 0 ... 1 0 1 ... 0	1	1	...	0	0	0	0	...	0	1
.....
0 1 0 ... 1 0 ... 0	1	0	...	0	0	0	0	...	1	1
1 0 ... 1 0 ... 0	0	0	0	...	0	0	0	1	...	1
1 1 ... 1 0 ... 0	0	0	0	...	0	0	1	1	...	1

We note that when $n - k = 1$ the faults corresponding to the contacts $(0, 0)_v$ and $(k, 0)_v$ are indistinguishable, since to them corresponds one and the same fault function

$$S_{n-1}(x_1, x_2, \dots, x_n) \vee x_1 x_2 \dots x_n.$$

It therefore remains to consider the case when $n - k$. Let us consider the $(n - k + 1)/2$ assemblies (the set T_4

$$\overbrace{1 1 1 \dots 1}^k 0 1 0 0 0 \dots 0,$$

$$0 0 1 \dots 1 1 1 0 1 0 \dots 0,$$

$$\dots \dots \dots \dots \dots \dots$$

Table 8

		$(1, l)_n$	$(2, l)_n$		$(k-2, l)_n$	$(k-1, l)_n$
	t					
$k = 2$	$n = h = t = 1$					
	0 . . . 0 1011 . . . 1 0 . . . 0	1	0	...	0	0
	0 . . . 0 1101 . . . 1 0 . . . 0	1	1	...	0	0
	0 . . . 0 1111 . . . 0 1 0 . . . 0	1	1	...	1	0
	0 . . . 0 1111 . . . 0 0 0 . . . 0	0	0	...	0	1
	$n = h = t$					

Here each succeeding assembly is obtained from the preceding one by shifting the ones to the right by two columns, with the exception of perhaps the last one (for odd $n = k$), when the ones are shifted to the right by one column. With these assemblies, the network has the form shown in Fig. 26. It is seen therefore that in the case when the extreme vertical contacts of the first strip are faulty, then if the circuit conducts with the 1-st assembly, then the contact $(0, 0)_v$ is faulty, and if the circuit does not conduct with the 1-st assembly, then the contact $(0, k)_v$ is faulty. If the extreme vertical contacts of the 2-nd strip are faulty, then if the network conducts with the 1-st assembly, then the

contact $(1, k)_v$ is faulty, and if the circuit does not conduct ^{with} ~~on~~ the 1-st assembly, then the contact $(1, 0)_v$ is faulty, etc. This completes the proof of the fact that $T = T_1, + T_2, + T_3, + T_4$ (for $n - k \leq 1$ we have T_4 empty) is a test.

Let us estimate the length t of the test T . For this purpose we recall that

$$t_1 = n - k,$$

$$t_2 = 2,$$

$$t_3 = \begin{cases} (n - k + 1)(k - 2), & k \geq 3, \\ 1, & k = 2, n = 3, \\ 2, & k = 2, n = 4, \end{cases}$$

$$t_4 \leq \left[\frac{n - k + 1}{2} \right] \quad (= \text{for } n - k > 1).$$

Thus

$$t \leq (n - k + 1)(k - 2) + (n - k) + \left[\frac{n - k + 1}{2} \right] + 2 \text{ at } k \geq 3. \quad (*)$$

If $n - k \geq 3$, then by making a change of variables $x_1 = \bar{y}_1, x_2 = \bar{y}_2, \dots, x_n = \bar{y}_n$, the function $S_k(x_1, x_2, \dots, x_n)$ goes into the function $S_{n-k}(y_1, y_2, \dots, y_n)$ and the network $\gamma_{n,k}$ goes into network $\gamma_{n,n-k}$.

For the network $\gamma_{n,n-k}$, it is possible to construct, as above, a single closing test $T = \{(\alpha_1, \alpha_2, \dots, \alpha_n)\}$ of length

$$t \leq (k + 1)(n - k - 2) + k + \left[\frac{k + 1}{2} \right] + 2 \text{ npn } n - k \geq 3. \quad (**) \quad$$

It is obvious that $T^* = \{(\bar{\alpha}_1, \bar{\alpha}_2, \dots, \bar{\alpha}_n)\}$ is a single test for closing for the network $\gamma_{n,k}$, with $t^* = t$.

If $k \geq 3$ and $n - k \geq 3$, we take that group of the tests for which the estimate (*) or (**) is lower.

We denote by m the number of fault functions (equal to the number of contacts); we obtain

$$m = k(n - k + 1) + (n - k)(k + 1) = 2k(n - k) + n.$$

We estimate the ratio of the length of the obtained test to the number of fault functions, i.e., to the length of the trivial test (see Chapter I, Sec. 5). We have

$$\frac{t}{m} \leq \frac{\frac{1}{2}m - n + \frac{3}{2}k + \frac{1}{2}}{m} \quad \text{if } k \geq 3,$$

$$\frac{t}{m} \leq \frac{\frac{1}{2}m + \frac{n}{2} - \frac{3}{2}k + \frac{1}{2}}{m} \quad \text{if } n - k \geq 3.$$

Since the cases $k = 1$ or $n - k = 1$ are trivial, we shall assume that $k \geq 2$ and $n - k \geq 2$.

The expression $(-n + 3k/2 + 1/2)/m$, where $k \leq n - 2$, reaches a maximum when $k = n - 2$. In fact, in this case the numerator will have a maximum and the denominator a minimum. Analogously, the expression $(n/2 - 3k/2 + 1/2)/m$, where $k \geq 2$, reaches a test maximum $k = 2$. Thus

$$\frac{-n + \frac{3}{2}k + \frac{1}{2}}{m} < 0,1 \text{ and } \frac{\frac{n}{2} - \frac{3}{2}k + \frac{1}{2}}{m} < 0,1.$$

Consequently, when $\min(k, n - k) > 1$ we have $t/m < 0.6$

The preceding theorem gives a way of constructing a single closing test for elementary symmetrical functions $S_{n,k}$, realized by means of the networks $\gamma_{n,k}$. The natural question arises, however, of how "good" the constructed test is, i.e., in other words, how strongly the length of the constructed test differs from the length of the minimal test. Here we shall not give a complete answer to this question. For the case of symmetrical functions $S_{n,n-1}$ we shall propose a method of constructing a minimal test.* From this it is already easy to obtain a desired comparison and to conclude that the previously constructed tests are completely satisfactory.

* We have in mind the networks $\gamma_{n,n-1}$.

Theorem. For networks $\gamma_{n,n-1}$ the length t_{\min} of a single minimal test for closing T_{\min} , is equal to $q_n - [q_n/3] + 1$, where $q_n = 2(n - 1)$ is the number of horizontal contacts of the network $\gamma_{n,n-1}$.

Proof. We shall show first that $t_{\min} \geq q_n - [q_n/3] + 1$. We note first that the fault functions corresponding to the first and last vertical contacts are identically equal, i.e., $f_{00}^V = f_{0k}^V$ (see p. 313 of source7). It is further evident that to

establish faults in the extreme vertical contacts it is necessary to take the assembly $\alpha^0 = (1, 1, \dots, 1)$.

This assembly makes it possible to distinguish the case when a vertical contact is out of order from the case when either a horizontal contact is out of order or the network is in working order. Thus, $T_{\min} \supset \alpha^0$.

Let furthermore $T' \subset T_{\min}$, where T' is the test for faults in the horizontal contacts. By virtue of the preceding remark one can assume that $\alpha^0 \notin T'$. We denote by t'_{\min} the length of the minimal unit test for closing in the case when only the horizontal contacts can be faulty. We then have the following inequalities for the length t' of the test T' :

$$t_{\min} \geq t' + 1 \geq t'_{\min} + 1.$$

For the network $\mathcal{Y}_{n,n-1}$ (Fig. 27), the fault functions are tabulated in Table 9.

Note. The assemblies α^0 , $\alpha_j^1 (j \leq i)$ and also the functions f_C^h , f_{i0}^h , f_{j1}^h , and f_{k0}^v from the table for the network $\mathcal{Y}_{n,n-1}$ are identical with the corresponding assemblies and functions from the table for the network $\mathcal{Y}_{n',n'-1}$ for $n' \geq n$. The validity of this identification is connected with the fact that both tables are identical within the limits of the first $n + 1$ boxes.

Table 9 consists of n boxes, the construction of which, starting with the first, has quite definite regularity. We shall agree to denote the assemblies by α_j^i , where the superior index denotes the box to which the given assembly belongs and the inferior index denotes the number of the given assembly in the box, starting with the uppermost. Let us examine the part of Table 9, corresponding to the horizontal contacts. It is easy to see that this part of the table satisfies the following requirements:

- 1) Each row contains exactly two ones;
- 2) There are no identical rows or columns;
- 3) There exists one one function f_0 , to which corresponds a column containing no ones.

Let f_1 be an arbitrary fault function from the considered subtable, with $f_1 \neq f_0$. It is obvious that one of the assemblies on which the function f_1 assumes a value 1, should enter in the test. We denote this by α_1 . By virtue of property 1, we find in the subtable a function f_2 that assumes a value of 1 with the assembly 1. Let us consider a set of all such assemblies, on which $f_1 = 1$ or $f_2 = 1$. Let α_2 ($\alpha_2 \neq \alpha_1$) be an element of that set which enters into the test -- such an element will always be found, since $f_2 \neq f_1$, and by definition the test contains an assembly which distinguishes the

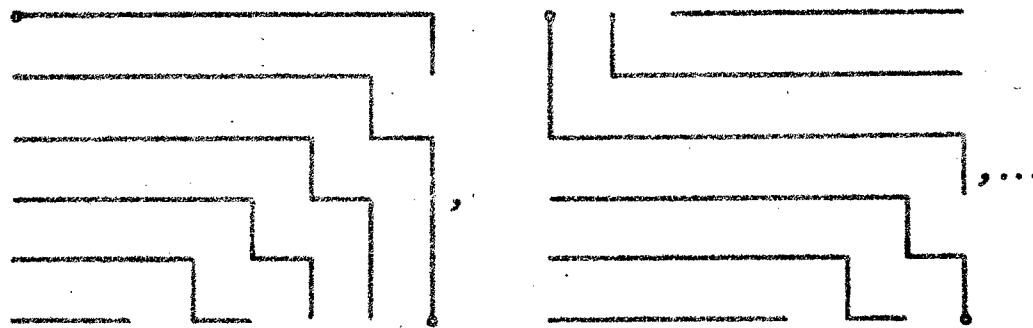


Fig. 26

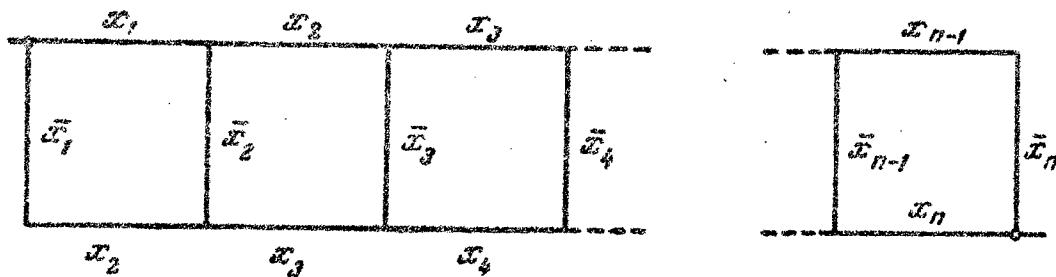


Fig. 27

	f_1	f_2	f_3
α_1	1	1	
α_2		1	1

Fig. 28

Table 9

No. HAO.	Assemblies						f_0	Horizontal Contacts								Vertical Contacts					$\frac{c}{c_1}$	No. boxes		
	x_1	x_2	x_3	x_4	x_5	\dots		f_{00}^r	f_{10}^r	f_{20}^r	f_{30}^r	\dots	f_{01}^r	f_{11}^r	f_{21}^r	f_{31}^r	\dots	f_{00}^u	f_{10}^u	f_{20}^u	f_{30}^u	f_{40}^u	\dots	
x^0	1	1	1	1	1	\dots						\dots					\dots	1	1	1	1	1	\dots	0
x_1^1	0	0	1	1	1	\dots		1				\dots	1				\dots						\dots	1
x_1^2	0	1	0	1	1	\dots		1				\dots	1				\dots	1					\dots	2
x_2^2	1	0	0	1	1	\dots			1			\dots	3				\dots						\dots	
x_1^3	0	1	1	0	1	\dots		1	.			\dots		1			\dots	1	1				\dots	
x_2^3	1	0	1	0	1	\dots			1			\dots		1			\dots		1				\dots	8
x_3^3	1	1	0	0	1	\dots				1		\dots			1		\dots						\dots	
x_1^4	0	1	1	1	0	\dots		1				\dots			1		\dots	1	1	1			\dots	
x_2^4	1	0	1	1	0	\dots			1			\dots			1		\dots		1	1			\dots	4
x_3^4	1	1	0	1	0	\dots				1		\dots			1		\dots			1			\dots	
x_4^4	1	1	1	0	0	\dots					1	\dots				1	\dots						\dots	

functions f_1 and f_2 (it follows, incidentally, from the properties 1 and 2 that on any assembly different from α_1 and contained in this set, the functions f_1 and f_2 are distinguishable, i.e., they assume opposite values). It follows from property 1 that there exists a function f_3 such that it assumes the value 1 on the assembly α_2 . Consequently, on the assemblies α_1 and α_2 the functions f_1 , f_2 , and f_3 are completely distinguishable (Fig. 28), and the corresponding faults are detected. It is obvious that these assemblies do not break down in any manner the remaining set of functions of the investigated part of the table. We cross out from the table the columns corresponding to the functions f_1 , f_2 , and f_3 as well as the rows corresponding to the assemblies α_1 and α_2 .

In the remaining table there can appear identical rows, and in the successive steps also rows which do not contain ones. Let us perform the following operations on the table: 4)-

- 1) We leave only one representative for each of the identical rows;
- 2) We cross out entirely the rows which do not contain ones.

We then obtain a table which need no longer satisfy requirement 1, for it may contain rows which contain a single one each. Let us take arbitrarily

the function f_4 from the table. One of the assemblies, with which it assumes the value of 1, should enter into the test. With this, two cases are possible.

a) There exists only one assembly with which the function is equal to 1, and the row corresponding to this assembly contains only one 1. Such an assembly must enter in the test; on it only one function is defined.

b) There exist rows (or a row) corresponding to assemblies, with which the investigated function is equal to 1, and containing two ones.

Using arguments, similar to those made for regarding f_1 , the function f_4 we either separate three functions, which are distinguishable completely with the

two assemblies, or else, if this can be done, we define two functions that are distinguishable with the two assemblies.

(There are no other possibilities,

for in none of the steps can identical columns occur).

From this we see that violation of condition 1 can lead only to an increase in the test compared with the ideal case, when for each step condition 1 is satisfied.

Since the initial part of the table (for the horizontal contacts) contains $q_n = 2(n - 1)$ functions, we obtain the following estimate

$$t_{\min} \geq \left[\frac{q_n}{3} \right] \cdot 2 + q_n - \left[\frac{q_n}{3} \right] 3 = q_n - \left[\frac{q_n}{3} \right].$$

The presence of the term $q_n - \left[q_n/3 \right] 3$ is due to the need for distinguishing between the remaining $q_n - \left[q_n/3 \right] 3$ functions and f_0 . For this purpose it is necessary to have $q_n - \left[q_n/3 \right] 3$ assemblies. This proves that

$$t_{\min} \geq q_n - \left[q_n/3 \right] + 1.$$

It now remains to show that $t_{\min} \leq q_n - \left[q_n/3 \right] + 1$. For this purpose we construct a test of length $q_n - \left[q_n/3 \right] + 1$. The construction and the proof will be carried out by induction with respect to n . To facilitate further considerations we formulate the property of the test T_n (see Table 9) in the following manner.

1. $\alpha^0 = (1, \dots, 1)$, $\alpha_1^1 = (001 \dots 1) \in T_n$.

..

2. From each box \mathbf{f} (starting with the second), T_n contains at least one assembly $\alpha_{i_f}^f$, where $i_f < f$.

3. a) If $q_n = 3k$, then the test T_n contains the assemblies α_{n-1}^n and α_n^n , and with these assemblies the functions $f_{n-2,0}^h$, $f_{n-1,0}^h$, and $f_{n-1,1}^h$ are distinguishable.

- b) If $q_n = 3k + 1$, then $\alpha_n^n \in T_n$ and only the function $f_{n-1,0}^h$ is determined with the assembly α_n^n (the other functions are determined with the remaining assemblies).

- c) If $q_n = 3k + 2$, then the test T_n contains the assemblies α_{n-2}^n , α_{n-1}^n , and α_n^n , and with these assemblies

α_{n-1}^n and α_n^n one determines only the functions $f_{n-2,0}^h$ and $f_{n-1,0}^h$.

The first step in the induction if for $n = 3$ ($q_3 = 3 + 1$). From Table 9 it is easy to establish that the set

$$T_3 = \{x^0, x_1^1, x_1^0, x_2^0\}$$

is a test. It is easy to verify that T_3 has properties 1, 2, and 3b).

Assume that the tests T_3, \dots, T_{n-1} ($n \geq 3$) with properties 1--3 inclusive have already been constructed; we shall show how to construct the test T_n . According to the different residues obtained by dividing q_{n-1} by 3, we consider three cases.*

* When estimating the lower bound (see p. 318 [of source]) we have seen that the consideration depends on the residue obtained by dividing q_n by 3.

a) $q_{n-1} = 3k$. We put

$$T_n = T_{n-1} - x_{n-1}^n + x_{n-2}^n + x_{n-1}^n + x_n^n.$$

From this we see that T_n differs from T_{n-1} by the assemblies from boxes $n - 1$ and n . We consider part of Table 9 corresponding to these boxes (Table 9a).

Table 9a

	...	$f_{n-3,0}^r$	$f_{n-2,0}^r$	$f_{n-1,0}^r$...	$f_{n-3,1}^r$	$f_{n-2,1}^r$	$f_{n-1,1}^r$
...
α_{n-3}^{n-3}	...	1	1	.
α_{n-1}^{n-1}	1	1	.
...
α_{n-2}^n	...	1	1
α_{n-1}^n	1	1
α_n^n	1	1

It is clear from Table 9 (see p. 317 [of source]) that T_{n-1} , being a test for the network $\mathcal{Y}_{n-1,n-2}$, distinguishes completely the functions $f_{00}^h, \dots, f_{n-2,0}^h$ and $f_{01}^h, \dots, f_{n-1,1}^h$, considered as fault functions for the network $\mathcal{Y}_{n,n-1}$, and by the induction assumption, the functions $f_{n-3,0}^h, f_{n-2,0}^h$ and $f_{n-2,1}^h$ are completely determined with the assemblies α_{n-2}^{n-1} and α_{n-1}^{n-1} . It is obvious that with the assemblies $\alpha_{n-2}^{n-1}, \alpha_{n-2}^n, \alpha_{n-1}^n$, and α_n^n (see Table 9a) determine completely the functions $f_{n-3,0}^h, f_{n-2,0}^h, f_{n-1,0}^h, f_{n-2,1}^h$ and $f_{n-1,1}^h$.

It is clear that T_n has properties 1 and 2. In fact, property 1 is satisfied in a trivial manner. Since α_{n-2}^{n-1} and $\alpha_{n-2}^n \in T_n$, and since T_n coincides with T_{n-1} on the boxes $l < n-1$, whereas for T_{n-1} property 2 is satisfied, then T_n has property 2. It is seen from Table 9 that the set T_n , which satisfies requirements 1 and 2, ^{makes} the faults in the vertical contacts completely localized. Finally, if we have T_n identically 0, then the network is in working order.

We have proved thus that T_n is a test. Since $q_n = 3k + 2$, it is necessary to establish that T_n also has property 3c. It follows from Table 9a that the functions $f_{n-3,0}^h$, $f_{n-2,1}^h$, and $f_{n-1,0}^h$ are determined ^{with} the assemblies α_{n-2}^{n-1} and α_{n-2}^n , while the functions $f_{n-2,0}^h$ and $f_{n-1,0}^h$ are determined ^{with} the assemblies α_{n-1}^n and α_n^n . The remaining functions are not distinguishable ^{with} these assemblies. Thus, 3c does take place.

b) $q_{n-1} = 3k + 1$. In this case we assume

$$T_n = T_{n-1} - \alpha_{n-1}^{n-1} + \alpha_{n-1}^n + \alpha_n^n.$$

Here, too, T_n differs from T_{n-1} in the assemblies from boxes $n-1$ and n . Using the fact that T_{n-1} is a test for $\gamma_{n-1,n-2}$ with properties 1-3b, and also using the fulfillment of properties 1 and 2 for T_n , we shall prove, analogously as in the item "a," that

T_n is a test for the network $\gamma_{n,n-1}$. Since $q_n = 3k + 3 = 3(k + 1)$, it is necessary to verify the fulfillment of item 3a. From the definition of T_{n-1} it follows that $T_{n-1} = \alpha_{n-1}^{n-1}$ determines all the functions (corresponding to the network $\gamma_{n-2,n-1}$), the only possible exception being $f_{n-2,0}^h$. It is easy to see, however, that with the assemblies α_{n-1}^n and α_n^n the functions $f_{n-2,0}^h$, $f_{n-1,0}^h$, and $f_{n-1,1}^h$ are completely distinguishable. All the remaining functions coincide with these assemblies. This proves the fulfillment of item 3a.

c) $q_{n-1} = 3k + 2$. We put

$$T_n = T_{n-1} - \alpha_{n-2}^{n-1} - \alpha_{n-1}^{n-1} + z_{n-2}^* + z_{n-1}^* + z_n^*.$$

Obviously, T_n has property 1. Since T_n corresponds with T_{n-1} on the boxes $\ell < n - 1$, and since T_{n-1} fulfills requirement 2, then, considering that α_{n-3}^{n-1} and $\alpha_{n-2}^n \in T_n$, we conclude that T_n has property 2. Using the fact that T_{n-1} is a test for $\gamma_{n-1,n-2}$ and that T_n has properties 1 and 2, let us prove, as in item "a," that T_n is a test for the network $\gamma_{n,n-1}$. Since $q_n = 3k + 4 = 3(k + 1) + 1$, it remains to verify the fulfillment of item 3b. In fact, by the induction assumption, $T_{n-1} = \alpha_{n-2}^{n-1} - \alpha_{n-1}^{n-1}$ determine all the functions $f_{00}^h, \dots, f_{n-4,0}^h, f_{01}^h, \dots, f_{n-2,1}^h, f_{00}^v, \dots, f_{n-1,0}^v$,

and the functions $f_{n-3,0}^h$ and $f_{n-2,0}^h$ are distinguished with the assemblies α_{n-2}^{n-1} and α_{n-1}^{n-1} . It is clear that the functions $f_{n-3,0}^h$, $f_{n-2,0}^h$, and $f_{n-1,1}^h$ are fully determined with the assemblies α_{n-2}^n and α_{n-1}^n , which are added to T_{n-1} in place of the assemblies α_{n-2}^{n-1} and α_{n-1}^{n-1} . Finally, the function $f_{n-1,0}^h$ is determined with the assembly α_n^n . Thus, item 3b is satisfied for T_n .

It now remains to verify that T_n has a length

$$t_n = q_n - \lceil q_n/3 \rceil + 1. \text{ In fact, } t_3 = 4 = 4 - \lceil 4/3 \rceil + 1 = q_3 - q_3/3 + 1. \text{ Let us put } t_{n-1} = q_{n-1} - q_{n-1}/3 + 1. \text{ We shall show that } t_n = q_n - \lceil q_n/3 \rceil + 1. \text{ For this}$$

purpose we consider three cases:

a) $q_{n-1} = 3k$,

$$t_n = t_{n-1} + 2 = q_{n-1} - \left\lceil \frac{q_{n-1}}{3} \right\rceil + 1 + 2 = q_{n-1} + 2 - \left\lceil \frac{q_{n-1} + 2}{3} \right\rceil + 1 = q_n - \left\lceil \frac{q_n}{3} \right\rceil + 1;$$

b) $q_{n-1} = 3k + 1$,

$$t_n = t_{n-1} + 1 = q_{n-1} - \left\lceil \frac{q_{n-1}}{3} \right\rceil + 1 + 1 = q_{n-1} + 2 - \left\lceil \frac{q_{n-1} + 2}{3} \right\rceil + 1 = q_n - \left\lceil \frac{q_n}{3} \right\rceil + 1;$$

c) $q_{n-1} = 3k + 2$,

$$t_n = t_{n-1} + 1 = q_{n-1} - \left\lceil \frac{q_{n-1}}{3} \right\rceil + 1 + 1 = q_{n-1} + 2 - \left\lceil \frac{q_{n-1} + 2}{3} \right\rceil + 1 = q_n - \left\lceil \frac{q_n}{3} \right\rceil + 1.$$

This completes the proof of the theorem. It is necessary to indicate here that the theorem not only establishes the existence of tests with different properties, but also gives a very effective method of

their construction, which does not require the scanning of all the subsets of the sets of n -term assemblies.

7. Test for a Network that Realizes a Linear Function

The function $\Phi(x_1, x_2, \dots, x_n)$ of algebraic logic is called linear,* if the following representation takes place

$$\Phi(x_1, x_2, \dots, x_n) = A_0 + A_1 x_1 + \dots + A_n x_n \pmod{2}.$$

Knowing the network realization of the function

$$\Phi_0(x_1, x_2, \dots, x_n) = n + x_1 + x_2 + \dots + x_n \pmod{2},$$

it is easy to obtain a network realization of any linear function, which depends on more than n arguments. It is known [7] that $\Phi_0(x_1, x_2, \dots, x_n)$ can be realized by means of the network \mathcal{Q}_n (Fig. 29). We see that this network is made up of blocks of the form shown in Fig. 30.

* For a linear function one encounters also in the literature the term the "parity counter."

In the present section we shall give a method of constructing test for the network \mathcal{Q}_n . We shall prove here the following statement.

Theorem. For a network \mathcal{O}_n , realizing a linear function $\Phi_0(x_1, x_2, \dots, x_n)$, it is possible to construct a single test T_n of length $t_n \leq 3n - 2$.

We note that the closing of contact 1 and the closing of contact 2 of the i -th block ($i \geq 3$) gives one and the same fault function. In fact, when contact 1 is closed, then there is a circuit 3--1--4 connected in parallel with contact 2, and this circuit has an admittance \bar{x}_i , i.e., it produces the same effect as if contact 2 were also closed, and vice versa. It is established analogously that closing of contact 3 and the closing of contact 4 corresponds to one and the same fault function. Furthermore, the differences in all the remaining fault functions will follow from the fact, which is about to be established, that all the indicated faults are localized.

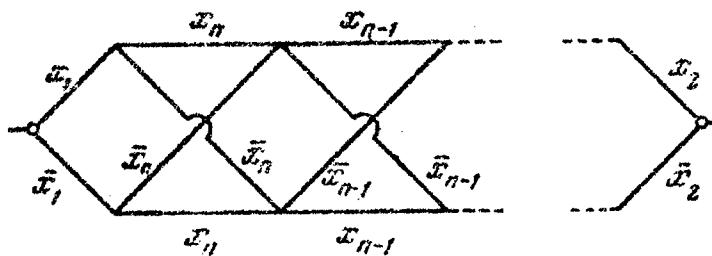


Fig. 29

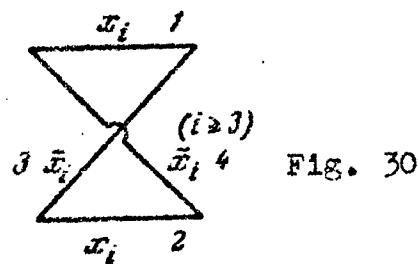


Fig. 30

We prove the theorem by induction with respect to n . In the particular case $n = 2$, the set $T_2 = \{(00), (01), (10), (11)\}$ is a test (trivial; see introduction). In this case the following faults cannot be distinguished:

opening of contact x_1 and opening of contact x_2

" " " x_1 and " " " x_2

closing of contact x_1 and closing of contact x_2

" " " x_1 and " " " x_2

Let $n = 3$ (first step of the induction). It is seen from Table 10 of the fault functions of network Ω_3 that $T_3 = \{(001), (011), (101), (111), (000), (010), (100)\}$ is a test that distinguishes all the faults contained in the table.

We introduce the notation $\delta' = ((\delta, 1))$, where $\delta = (\delta_1, \delta_2, \dots, \delta_n)$, i.e., $\delta' = (\delta_1, \delta_2, \dots, \delta_n, 1)$. If Δ is the set of assemblies δ , then $\Delta' = ((\Delta, 1))$ is the set of assemblies $\delta' = ((\delta, 1))$.

We put

$$\begin{aligned} \text{for } n = \text{even} \quad & \left\{ \begin{array}{l} \alpha_n = (0, 0, 0, \dots, 0), \\ \beta_n = (1, 1, 0, \dots, 0), \\ \gamma_n = (0, 1, 0, \dots, 0); \end{array} \right. \\ \text{for } n = \text{odd} \quad & \left\{ \begin{array}{l} \alpha_n = (0, 1, 0, \dots, 0), \\ \beta_n = (1, 0, 0, \dots, 0), \\ \gamma_n = (0, 0, 0, \dots, 0). \end{array} \right. \end{aligned}$$

Table 10

$(x_1 x_2 r_3)$	Φ_0	Short						Break					
		1st bl.	2nd bl.	3rd bl.	1st bl.	2nd bl.	3rd bl.	x_1	\bar{x}_1	x_2	\bar{x}_2	r_1	\bar{r}_1
(000)	0	1	1	1									
(011)	0	1		1									
(101)	0		1	1									
(110)	0		1		1								
(111)	1											0	0
(010)	1							0	0			0	0
(100)	1							0	0			0	0
(111)	1							0	0			0	0

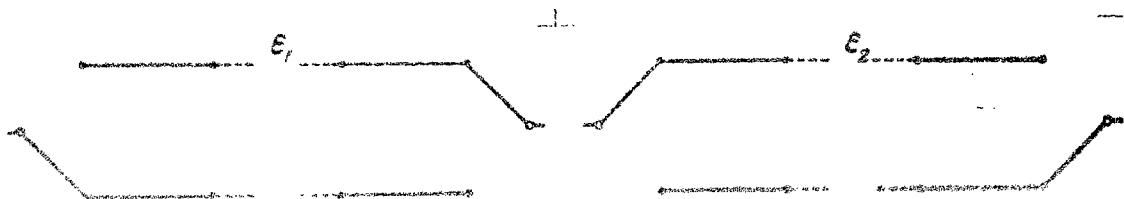


Fig. 31

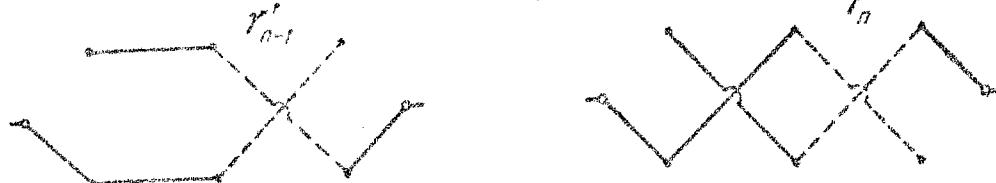


Fig. 32

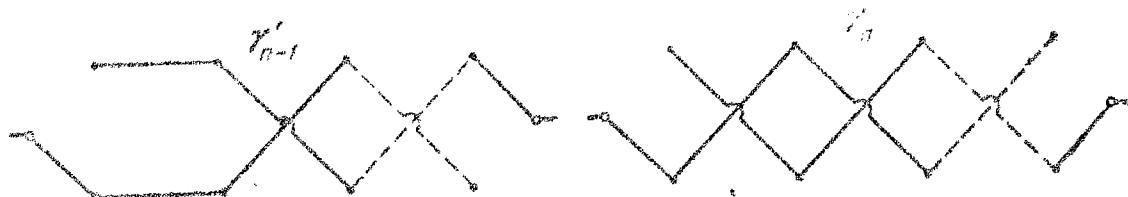


Fig. 33

Second Step of Induction. Let there be constructed tests T_k for the networks \mathcal{N}_k , where $k < n$, and let the length of the test T_k be $t_k \leq 3k - 2$. We define

$$T_n := \{(T_{n-1}, 1), z_n, \beta_n, \gamma_n\}.$$

It is clear that $t_n \leq 3(n-1) - 2 + 3 = 3n - 2$. Let us prove that T_n is a test. We note that from the definition of T_n it follows that the test contains the assemblies $\epsilon_1 = (0, 1, 1, \dots, 1)$ and $\epsilon_2 = (1, 0, 1, \dots, 1)$. We first indicate how to detect the fault in

the n -th block (if such exists). Since the network Ω_n assumes with the assemblies ε_1 and ε_2 the form shown respectively in the left and the right parts of Fig. 31, we have for $\Phi_0(\varepsilon_1) \neq \Phi_0(\varepsilon_2)$ a short circuit in the 1-st or in the 2-nd block. Therefore in the 1-st and 2-nd blocks there is no short circuit if $\Phi_0(\varepsilon_1) = \Phi_0(\varepsilon_2)$. In the case when there is no short circuit in the 1-st and 2-nd blocks, a further investigation is necessary. Let us consider further the assemblies

$$\gamma_{n-1} = (0, \eta, 0, \dots, 0, 1) \text{ and } \gamma_n = (0, \bar{\eta}, 0, \dots, 0).$$

It is obvious that the appearance of the network Ω_n with these assemblies depends on the evenness of n .

When n is even it has the form shown in Fig. 32, and when n is odd it has the form shown in Fig. 33. Analyzing these cases we reach the conclusion that one of the contacts 1 or 2 (in the n -th block) is shortcircuited if $\Phi_0(\gamma'_{n-1}) = 0$ and $\Phi_0(\gamma_n) = 1$, and that one of the contacts 3 or 4 is shortcircuited if $\Phi_0(\gamma'_{n-1}) = 1$ and $\Phi_0(\gamma_n) = 0$. If, however, $\Phi_0(\gamma'_{n-1}) = \Phi_0(\gamma_n)$, then there is no closing in the n -th block.

It now remains to provide a prescription for detecting open circuits in the n -th block. For this purpose we examine the network Ω_n on the assemblies $\alpha_n, \beta_n, \alpha'_{n-1}, \beta'_{n-1}$ (Fig. 34). Since the networks

"a" and "c" coincide only in the link x_1 , then when $\Phi_0(\alpha_n) \neq \Phi_0(\alpha'_{n-1})$, the contact x_1 cannot be open; analogously, from the fact that the networks "b" and "d" coincide only on the link x_1 , we conclude that when $\Phi_0(\beta_n) \neq \Phi_0(\beta'_{n-1})$ the contact x_1 cannot be open.

Next, comparing networks "a" and "d" with "b" and "c" respectively, we see that the foregoing networks coincide pairwise in all blocks, with the exception of the 1-st and the n-th. From this we reach the conclusion that when $\Phi_0(\alpha_n) \neq \Phi_0(\beta'_{n-1})$ or respectively $\Phi_0(\beta_n) \neq \Phi_0(\alpha'_{n-1})$, there is an open circuit in the 1-st or in the n-th block. Since we have just provided a prescription for establishing an open circuit in the first block, the open circuit in the n-th block is detected; with this, if $\Phi_0(\alpha_n) = 0$, then contact 3 is open, if $\Phi_0(\beta_n) = 0$ then contact 4 is open, if $\Phi_0(\alpha'_{n-1}) = 0$, then contact 2 is open, and if $\Phi_0(\beta'_{n-1}) = 0$, then contact 1 is open. This completes the analysis of the n-th block. If the n-th block is in working order, we put $x_n = 1$ and the network Ω_n goes into Ω_{n-1} . With this, there is a mutually unique correspondence between the assemblies from $((T_{n-1}, 1))$ and the assemblies from T_{n-1} . Since, by the induction assumption, T_{n-1} is a test for Ω_{n-1} , we can monitor the network Ω_{n-1} .

completely, i.e., we can monitor all blocks from 1 to $n - 1$ inclusive. If it is found that the subnetwork \mathcal{O}_{n-1} is in working order, this means that the entire network \mathcal{O}_n is in working order. This proves the theorem completely.

In conclusion, we get tests for $n = 4$ and $n = 5$:

$$T_4 = \{(0011), (0111), (1011), (1111), (0001), (0101), (1001), (0000), (0100), (1100)\},$$

$$T_5 = \{(00111), (01111), (10111), (11111), (00011), (01011), (10011), (00001), (01001), (11001), (00000), (01000), (10000)\}.$$

It is easy to verify that the algorithm proposed above for the construction of tests of the network \mathcal{O}_n , gives for $n = 3, 4$, and 5 minimal tests.

8. Test for the Comparison Network

Of particular interest is the comparison network, i.e., a network which realizes the function

$$f(A, B) = \begin{cases} 1 & \text{for } A \leq B, \\ 0 & \text{for } A > B. \end{cases}$$

Thus, let $A = a_n a_{n-1} \dots a_1$ and $B = b_n b_{n-1} \dots b_1$ be two n -^{bit} _{column} binary numbers, and then

$$f(a_n, \dots, a_1; b_n, \dots, b_1) = \bar{a}_n b_n \vee (\bar{a}_n b_n \vee a_n b_n) f^{-1}(a_{n-1}, \dots, a_1; b_{n-1}, \dots, b_1) = = \bar{a}_n b_n \vee (\bar{a}_n b_n \vee b_n) f^{-1}(a_{n-1}, \dots, a_1; b_{n-1}, \dots, b_1).$$

This function can be realized by the network shown in Fig. 35.* Thus, the comparison network \mathcal{O}_n consists of the $(n - 1)$ -th block of the form shown in Fig. 36, and one block shown in Fig. 37. With this, the blocks are joined in the manner as shown in Fig. 38. The network given contains $4n - 2$ contacts.

The next problem is the construction of a minimal single test for the comparison network. Here we become acquainted with another use of the block structure of the network for the construction of a test. The method proposed consists of constructing the test for the entire network of tests for individual blocks. Thus, the block nature of the network is used in an entirely different manner than was done in Sec. 7, where the block structure was taken into account essentially in the law of construction of the test, and also in the inductive proof. However, such a law of construction of the test was to a considerable extent, so to speak, "guessed at", more accurately, so to speak, "noted"; here, to be sure in embryonic form, we propose a principle of constructing tests for block networks.

Theorem. The minimal single test T_n for a comparison network \mathcal{O}_n has a length $t_n = 2n + 4(n > 2)$.**

Proof. We make up tables of functions of faults of the 1-st block (Table 11), and also of the i -th block

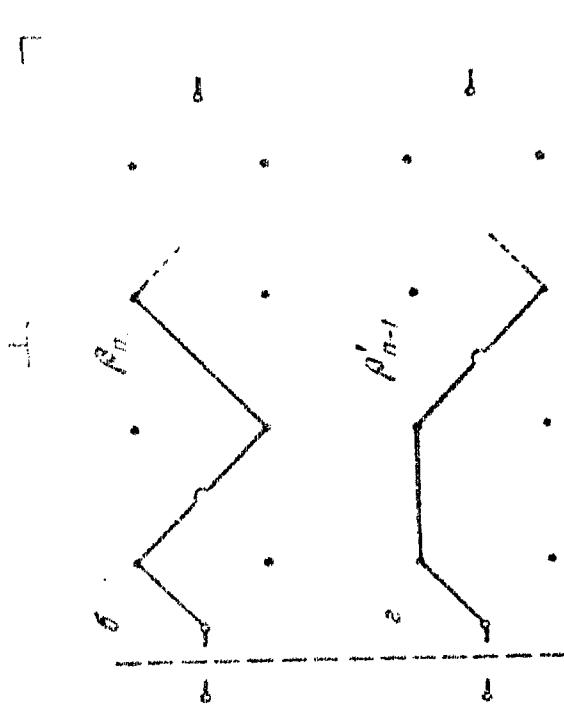


Fig. 34

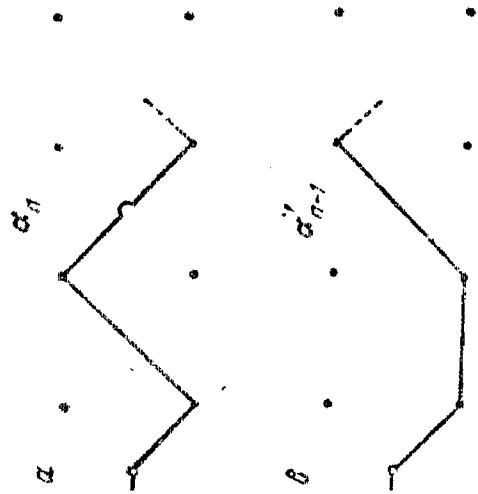
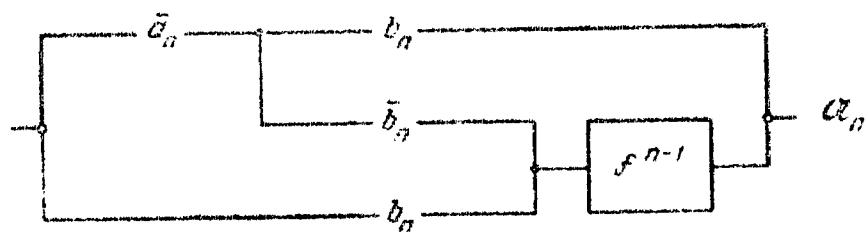
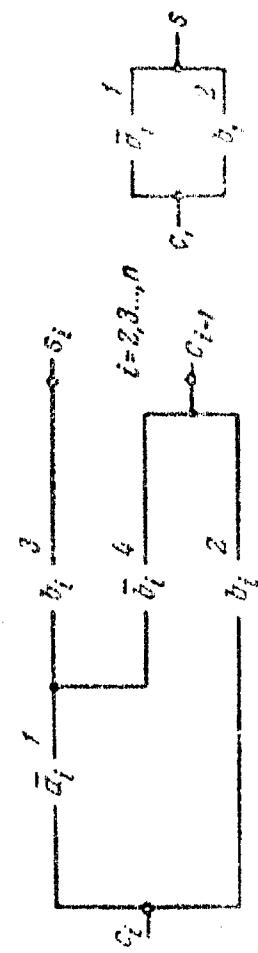


Fig. 35



106



36



$(1 \leq i \leq n)$ (Table 12), considered as a multi-terminal network with one input and two outputs. For the i -th block, the values of the functions are written in decimal system, starting with dual notation s_{i-1}^c .

* The network given here is simpler than that constructed in reference /3/ by G. N. Povarov by the cascade method.

** Obviously, $t_1 = 3, t_2 = 7$.

The i -th block is connected in the network in the manner shown in Fig. 39. From this we have the following:

a) If $c_{i-1} = 0$, for example, $a_i = 1, b_i = 0$, then all the circuits passing through subnetwork \mathcal{L} , are open, and therefore the operation of the subnetwork \mathcal{L} cannot be verified with such assemblies.

b) If $s = 1$ (in the i -th block), then $a_i = 0, b_i = 1$, the subnetwork \mathcal{L} is blocked, and therefore under our conditions the operation of subnetwork \mathcal{L} also cannot be verified.

c) No matter what the state of subnetwork \mathcal{L} , we cannot distinguish between the two states of the remaining part of the network, namely when $s = 1, c_{i-1} = 0, s = 1, c_{i-1} = 1$ (i.e., we do not distinguish between the

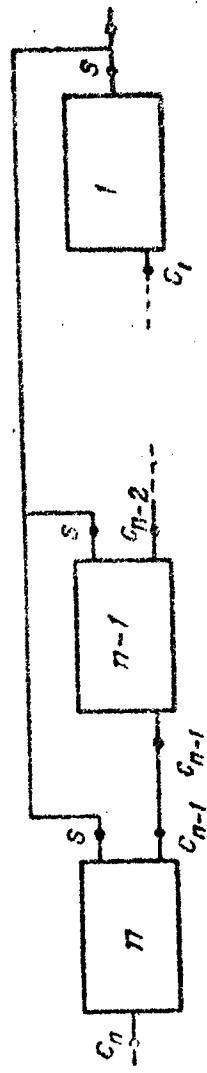


Fig. 38

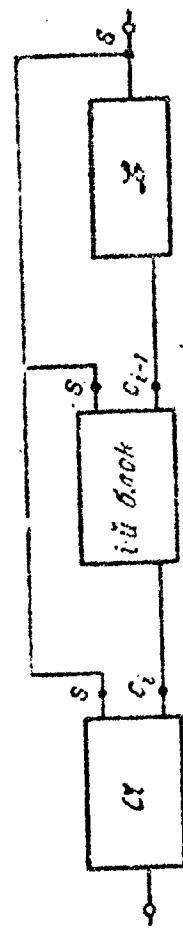


Fig. 39

values of the functions 2 and 3). The remaining combinations of the states s_{i-1} are pairwise distinguishable. Therefore a table of fault functions for the i -th block connected in the network can be written in the form of Table 13.

Table 11 shows that the minimal test for the first block consists of three assemblies $(0, 0)$, $(1, 0)$, and $(1, 1)$; from Tables 12 and 13 we obtain one and the same minimal test for the i -th block ($i > 1$), consisting of all four possible assemblies. One must note here, however, that in the construction of a test for the i -th block ($i > 1$), we begin from the fact that on the assemblies $(0, 0)$ and $(1, 1)$ we used essentially information on the outputs s and c_{i-1} , whereas in the verification of the i -th block, connected in the general network, we obtain information only from the output s . By virtue of this circumstance, we need for the verification of the i -th block not 4 assemblies, but more -- 6 assemblies (since 3 differs from 0, and also 4 differs from 0, only on the assembly $(0, 0)$; 4 differs from 0 and also 2, differs from 0, only on the assembly $(1, 1)$; then the assemblies $(0, 0)$, $(1, 1)$ must be taken both in the closed state and in the open state of the subset \mathcal{S}). For convenience we shall write

Table 11

$(a_1 b_1)$	0	1	2	1'	2'
(0, 0)	1			0	
(0, 1)	1				
(1, 0)	0	1	1		
(1, 1)	1				0

$$f_1 = f_2$$

Table 12

(a_1, b_1)	0	1	2	3	4	1'	2'	3'	4'
(0, 0)	1			3		0			0
(0, 1)	3					1	2	1	
(1, 0)	0	1	1						
(1, 1)	1	3			3		0		

Table 13

(a_1, b_1)	0	1	2	3	4	1'	2'	3'	4'
(0, 0)	1			2		0			0
(0, 1)	2					1		1	
(1, 0)	0	1	1						
(1, 1)	1	2			2		0		

the assemblies $(\alpha_n, \dots, \alpha_1; \beta_n, \dots, \beta_1)$ in the form

$\begin{pmatrix} \alpha_n, \dots, \alpha_i \\ \beta_n, \dots, \beta_i \end{pmatrix}$. From items a) and b) it follows

that with the aid of the assemblies $\begin{pmatrix} \alpha_n, \dots, \alpha_{i+1}, \alpha_i \\ \beta_n, \dots, \beta_{i+1}, \beta_i \end{pmatrix}$

one cannot monitor blocks $i = 1, 2, \dots, l$.

Since for each i ($i > 1$) there is at least one assembly with $\alpha_i = 1$ and $\beta_i = 0$, and at least one assembly with $\alpha_i = 0$ and $\beta_i = 1$, then the minimal test T_n must include the assemblies

$$\alpha' = \begin{pmatrix} \alpha'_n, \dots, \alpha'_{i+1}, 1, \dots \\ \alpha'_n, \dots, \alpha'_{i+1}, 0, \dots \end{pmatrix}, \quad \beta' = \begin{pmatrix} \beta'_n, \dots, \beta'_{i+1}, 0, \dots \\ \beta'_n, \dots, \beta'_{i+1}, 1, \dots \end{pmatrix}.$$

From the foregoing arguments and from item "c" it follows that to monitor the second block it is necessary that there be present assemblies with $\alpha_2 = \beta_2 = 0$, and $\alpha_2 = \beta_2 = 1$, both with $(\alpha_1, \beta_1) = (1, 0)$ and with $(\alpha_1, \beta_1) \neq (1, 0)$. Therefore the test T_n must contain the assemblies

$$\gamma' = \begin{pmatrix} \gamma'_n, \dots, \gamma'_3, 0, 1 \\ \gamma'_n, \dots, \gamma'_3, 0, 1 \end{pmatrix}, \quad \gamma'' = \begin{pmatrix} \gamma''_n, \dots, \gamma''_3, 1, 1 \\ \gamma''_n, \dots, \gamma''_3, 1, 0 \end{pmatrix},$$

$$\delta' = \begin{pmatrix} \delta'_n, \dots, \delta'_3, 0, \alpha_1^0 \\ \delta'_n, \dots, \delta'_3, 0, \beta_1^0 \end{pmatrix}, \quad \delta'' = \begin{pmatrix} \delta''_n, \dots, \delta''_3, 1, \alpha_1' \\ \delta''_n, \dots, \delta''_3, 1, \beta_1' \end{pmatrix}.$$

where

and

$$(\alpha_1^0, \beta_1^0) \neq (1, 0) \text{ and } (\alpha_1', \beta_1') \neq (1, 0).$$

Let us consider in greater detail the 1-st and 2-nd blocks of the network (Fig. 40). It is obvious that from among the foregoing assemblies only assemblies ξ' and ξ'' can participate in the analysis of opening of contacts 2 and 4 of the 2-nd block and contacts 1 and 2 of the 1-st block. Since the case that the network conducts both with assembly ξ' and with assembly ξ'' is possible with the network in working condition, one can recognize with the two assemblies ξ' and ξ'' at the most three faults (the fact that there are no coinciding fault functions for open circuits, follows from what will be given below). Thus, the test T_n should contain at least one more assembly ξ , different from those previously constructed. In the analysis of open circuits in the test, as we have seen, there should be present assemblies of the form γ' , γ'' and α^i ($i \geq 2$). Of these, only four are in the control of the first three blocks

$$\gamma' = \begin{pmatrix} \gamma_1', \dots, \gamma_n', 0, 1 \\ \gamma_1', \dots, \gamma_n', 0, 0 \end{pmatrix}, \quad \gamma'' = \begin{pmatrix} \gamma_1'', \dots, \gamma_n'', 1, 1 \\ \gamma_1'', \dots, \gamma_n'', 1, 0 \end{pmatrix},$$

$$\alpha^i = \begin{pmatrix} \alpha_1^i, \dots, \alpha_n^i, 1, \dots \\ \alpha_1^i, \dots, \alpha_n^i, 0, \dots \end{pmatrix}, \quad \alpha^i = \begin{pmatrix} \alpha_1^i, \dots, \alpha_n^i, 1, \dots \\ \alpha_1^i, \dots, \alpha_n^i, 0, \dots \end{pmatrix}.$$

We shall show that for any choice of values for γ_3^1 , γ_3^2 , and α_3^2 we cannot completely distinguish all the short-circuit faults for the 2-nd and the 3-rd blocks. Eight cases are possible here.

From item c it follows that when $\gamma_3^1 = \gamma_3^2 = \alpha_3^2$ the foregoing assemblies do not make it possible to monitor completely the third block. Thus, it remains to consider only those cases, when at least one of the number γ_3^1 , γ_3^2 , α_3^2 is equal to 0 and at least one is equal to 1.

If $\alpha_3^2 \neq \gamma_3^1 = \gamma_3^2$, then with the foregoing assemblies, when $\alpha_3^2 = 0$, we cannot distinguish short circuits of the 2-nd contact of the 2-nd block and the 3-rd contact of the 3-rd block, and when $\alpha_3^2 = 1$ we cannot distinguish open circuits of the 2-nd contact of the 2-nd block and the 4-th contact of the 3-rd block.

It remains to analyze the case when $\gamma_3^1 \neq \gamma_3^2$. Let γ_3^p denote that value of γ_3^1 , or γ_3^2 , which is different from α_3^2 . It is clear that with the assembly

$$\gamma = \begin{pmatrix} \gamma_n^p, \dots, \gamma_3^p, \gamma_2^p, 1 \\ \gamma_n^p, \dots, \gamma_3^p, \gamma_2^p, 0 \end{pmatrix}$$

the following pairs of faults cannot be distinguished from each other:

Star

#

1) when $\gamma_2^p = \gamma_3^p = 0$ -- closing of the 3-rd contacts of the 2-nd and the 3-rd blocks;

2) when $\gamma_2^p = 0, \gamma_3^p = 1$ -- closing of the 3-d contact of the 2-nd block and closing of the 4-th contact of the 3-rd block;

3) when $\gamma_2^p = 1, \gamma_3^p = 0$, -- closing of the 4-th contact of the 2-nd block and closing of the 3-rd contact of the 3-rd block;

4) when $\gamma_2^p = \gamma_3^p = 1$ -- closing of the 4-th contacts of the 2-nd and 3-rd blocks, and the corresponding faults are not monitored at all by the remaining two assemblies.

We have thus shown that in the case of closing it is necessary, in addition to the foregoing ones, to have at least one more assembly. Thus

$$t_n \geq 2(n-1) + 4 + 2 = 2n + 4.$$

Table 14

Gaps	Type of Faults	
	δ'	δ''
in the 2nd contact	1	0
in the 3rd contact	1	1
in the 1st or 4th contact	0	1

Table 15

1st possibility $f(\beta') = 1, f(\beta'') = 0^*$

Blocks	1st	2nd	3rd	4th	...	$(n-1)$ th	n -th
β	1	0	1	1	...	1	1
β^2	1	1	0	1	...	1	1
β^3	1	1	1	0	...	1	1
β^4	1	1	1	1	...	1	1
β^{n-2}	1	1	1	1	...	0	1
β^{n-1}	1	1	1	1	...	1	0

Table 16

2nd possibility $f(\beta') = f(\beta'') = 1$

Blocks	2nd	3rd	4th	5th	...	$(n-1)$ th	n -th
β^2	0	1	1	1	...	1	1
β^3	1	0	1	1	...	1	1
β^4	1	1	0	1	...	1	1
β^{n-1}	1	1	1	1	...	1	1
β^n	1	1	1	1	...	0	1

Table 17

Blocks Con- tacts	3rd possibility					4th possibility					5th possibility					6th possibility				
	1st	2nd	3rd	4th	5th	1	2	3	4	5	6	7	8	9	10	11	12	13	14	
2	0	1	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	
32	1	0	1	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	
33	1	1	1	0	1	1	0	0	0	0	0	0	0	0	0	0	0	0	0	
34	1	1	1	1	0	1	1	1	0	0	0	0	0	0	0	0	0	0	0	
...	
3n-2	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	
3n-1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	
3n	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	

It now remains to prove the inverse. For this we construct a test of length $2n+4$. We put*

$$T_s = \left\{ \begin{array}{l} \delta' = \begin{pmatrix} 0, \dots, 0, 0 \\ 0, \dots, 0, 0 \end{pmatrix}, \quad \delta'' = \begin{pmatrix} 1, \dots, 1, 1 \\ 1, \dots, 1, 1 \end{pmatrix}, \quad \gamma = \begin{pmatrix} 0, \dots, 0, 1 \\ 0, \dots, 0, 0 \end{pmatrix}, \\ \gamma'' = \begin{pmatrix} 1, \dots, 1, 1 \\ 1, \dots, 1, 0 \end{pmatrix}, \quad \epsilon = \begin{pmatrix} 0, \dots, 0, 1, 0 \\ 0, \dots, 0, 1, 0 \end{pmatrix}, \\ \beta^i = \begin{pmatrix} 0, \dots, 0, 1, 0^*, 1, \dots, 1 \\ 0, \dots, 0, 1, 1, 0, \dots, 0 \end{pmatrix} (i=2, \dots, n), \\ \alpha^i = \begin{pmatrix} 1, \dots, 1, 0, 1^*, 1, \dots, 1 \\ 1, \dots, 1, 0, 0, 1, \dots, 1 \end{pmatrix} (i=4, \dots, n) \end{array} \right\}.$$

* The asterisk denotes the i -th column.

Table 18

Short	Type of fault	
	γ'	γ''
1) в 1-м блоке	1	1
2) во 2-м контакте $i \geq 2$ блока	0	0
3) в 3-м контакте $i \geq 2$ блока	1	0
4) в 1-м или 4-м контакте $i \geq 2$ блока	0	1

KEY: 1) in the 1st block; 2) in the 2nd contact of the block $i \geq 2$; 3) in the 3rd contact of the block $i \geq 2$; 4) in the 1st and 4th contact of the block $i \geq 2$.

Table 19

2nd possibility $f(\gamma) = f(\gamma'') = 0$

	2nd bl	3rd bl	...	$(n-1)$ th bl	n-th bl
α^2	1	0	...	0	0
α^3	0	1	...	0	0
...
α^{n-1}	0	0	...	1	0
α^n	0	0	...	0	1

Table 20

3rd possibility $f(\gamma) = 1, f(\gamma'') = 0$

	2nd bl	3rd bl	...	$(n-1)$ th bl	n-th bl
α^1	1	0	...	0	0
α^2	0	1	...	0	0
...
α^{n-2}	0	0	...	1	0
α^{n-1}	0	0	...	0	1

Table 21

4th possibility $f(\gamma) = 0, f(\gamma'') = 1$

Blocks	2nd	3rd	4th	5th	...	$(n-2)$ th	$(n-1)$ th	n-th
Cont.	1	4	1	4	1	4	1	4
α^1	0	0	1	1	1	1	1	1
α^2	1	0	0	0	1	1	1	1
α^3	0	0	1	0	0	0	1	1
...
α^{n-2}	0	0	0	0	0	0	1	0
α^{n-1}	0	0	0	0	0	0	0	1
α^n	0	0	0	0	0	0	0	0

It is stated that T_n is a test. Let us analyze separately three cases:

I. The circuit does not conduct with at least one of the assemblies δ' , δ'' , ϵ , and β^i ($i = 2, \dots, n$).

In Table 14, depending on the states of the network with the assemblies δ' and δ'' we indicate several possibilities.

For further localization of the fault we make use of Tables 15--17. This completes the analysis of faults in the case of an open circuit.

II. At least with one of the assemblies γ' , γ'' , α^i ($i = 1, \dots, n$) the circuit conducts. The possibilities that are present here are indicated in Table 18. With the aid of Tables 19--21 we localize the fault in blocks $i \geq 2$. These tables make it possible to complete the analysis of the faults in the case of a closed circuit.

III. The network conducts with all the assemblies γ' , γ'' , ϵ , and β^i ($i = 2, \dots, n$), and it is open with all the assemblies γ' , γ'' , and α^i ($i = 1, \dots, n$). In this case the network is in working order. This proves the theorem completely.

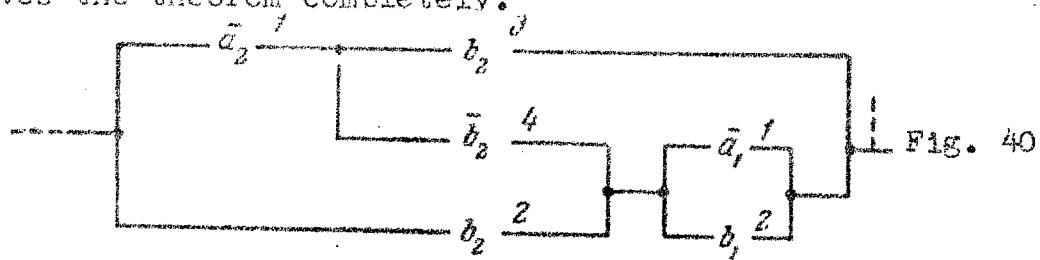


Fig. 40

9. Ordered and Tentative Tests.

Thus far we have considered principally the question of the procedure for constructing tests, without taking into account the specific nature of their utilization. It must be indicated here that in the monitoring of a network, we, first of all, test the assemblies in a definite order, and secondly, as a result of each test we obtain information concerning the state of the network.

An essential characteristic of a test is the time necessary to monitor the network. In this connection, particular significance attaches to the question of the construction of a minimal test, and also the question of the extent to which the test constructed deviates from a minimal one. However, as was indicated earlier (see Sec. 2), the verification time can be reduced also in a different manner, namely by rational utilization of the test already constructed.

Definition. An ordered test is the following system of verifying the network:

1. The test is broken down into groups, written out in a definite order (individual groups may contain also one element each).
2. After passing through each group of assemblies,

information is fixed regarding the state of the network.

3. If this information is sufficient to detect a fault, then further tests are discontinued, and in the opposite case, one proceeds to the next group.

It is seen even with simple examples that with such a system of running through the test, we can obtain the necessary information concerning the state of the network in individual cases (to detect a fault, for example), by running through only part of the entire test. An ordered test is characterized by a mathematical expectation of the length of the used part of the test. It is clear that corresponding to different arrangements of the group will be different values of mathematical expectations. It is therefore natural to strive for such an arrangement of the group, at which the minimum mathematical expectation is obtained.

When obtaining intermediate information it may turn out that in the remaining part of the test, the remaining assemblies will be superfluous, i.e., that running through these assemblies does not add to the information concerning the network. We shall analyze this circumstance in greater detail. For this purpose we introduce several symbols and definitions.

Assume that for a network Ω there is fixed a set of fault functions M and a set N of pairs of

fault functions in the sense of Sec. 2. We denote by T_0 a certain set of assemblies. It is obvious that as a result of running through the assemblies T_i we obtain information I_i concerning the network \mathcal{N} ($i = 1, 2, \dots, s_0$). The information I_i can be characterized by the function $\varphi_i(e)$, which assumes values 1 or 0 on the assembly $e \in T_0$, depending on whether or not the investigated network conducts with the assembly e . We note that the functions $\varphi_i(e)$ are specified only on the set

T_0 . We denote by \mathcal{M}_{I_i} the set of such functions $f_j(e)$ from \mathcal{M} , that $f_j(e) = \varphi_i(e)$ for $e \in T_0$.

This definition of the set \mathcal{M}_{I_i} can be decoded in the following manner. We arrange in some manner the assemblies from the set $T_0 = (e', e'', \dots)$. From the table of the fault functions \mathcal{M} we pick out those functions, which assume that the assembly e' a value $\varphi_i(e')$. From the resultant set we pick out further those functions, which assume a value $\varphi_i(e'')$ with the assembly e'' , etc.

Running through all the assemblies of the set T_0 , we obviously obtain \mathcal{M}_{I_i} .

We denote by \mathcal{M}_{I_i} the set of those pairs (f_j, f_k) from \mathcal{M} , for which f_j and $f_k \in \mathcal{M}_{I_i}$. Let T_{I_i} be the test corresponding to the set of the fault functions \mathcal{M}_{I_i} and to the set of the pairs of fault functions \mathcal{M}_{I_i} (T_{I_i} may prove to be empty).

Definition. A Tentative test T_y is called the following system for testing a network.

1. The set T_0 fixes the information I_i ($i = 1, 2, \dots, s_0$).

2. Depending on the information I_i obtained, further verification of the network is made with the aid of test T_{I_i} .

The tentative test is shown schematically in Fig. 41.

From the definition of the tentative test it follows directly that the set of assemblies $T = \{T_0, T_{I_1}, \dots, T_{I_{s_0}}\}$ is a test in the ordinary sense. Obviously, the construction given can be repeated many times.

Namely, if the information I_i does not give a complete answer concerning the state of the network, we take the set of assemblies T_1^i , where $T_1^i \cdot T_0 = N$. We then obtain supplementary information, etc., generally speaking until we obtain complete information concerning the state of the network. In this case, the tentative test is represented in the form of a "tree" (Fig. 42). Here the role of T_0 (see definition) is played by the tree. In particular, it may be found that each of the sets T_j^i consists of exactly one element.

For simplicity, we confine ourselves to an examination of the simplest tentative test, i.e., the case shown in Fig. 41.

Definition. The length of a tentative test T_t is called the quantity $t_t = \max(t_0 + t_{I_i}) = t_0 + \max t_{I_i}$, where t_{I_i} is the length of the test T_{I_i} .

It follows from the definition that it is possible to construct a tentative test T_y of length

$$t_y \leq t_{\min}.$$

For this purpose it is enough to take on T_0 the subset of T_{\min} , and to take for T_{I_i} the minimal test contained in $T_{\min} - T_0$. It is obvious that the form of the tentative test depends essentially on the choice of the set T_0 .

It remains unclear under what cases can one construct a tentative test T_y such that $t_y < t_{\min}$. The question also arises of whether there exist for any tentative test T_y of length $t_y \leq t_{\min}$ such a value of i , at which $t_0 + t_{I_i} < t_{\min}$.

We give an example of the construction of a tentative test.

Example. Tentative Test for the Comparison Network. Here we start out with the comparison network considered in Sec. 8.

We choose for T_0 the set of assemblies $\{\mathcal{E}', \mathcal{E}'', \mathcal{Y}', \mathcal{Y}''\}$, where again

$$\begin{aligned} v = & \begin{pmatrix} 0, \dots, 0, 0 \\ 0, \dots, 0, 0 \end{pmatrix}, \quad \delta' = \begin{pmatrix} 1, \dots, 1, 1 \\ 1, \dots, 1, 1 \end{pmatrix}, \quad \gamma = \begin{pmatrix} 0, \dots, 0, 1 \\ 0, \dots, 0, 0 \end{pmatrix}, \\ \gamma' = & \begin{pmatrix} 1, \dots, 1, 1 \\ 1, \dots, 1, 0 \end{pmatrix}. \end{aligned}$$

From the scheme and the tables we have the following:

- 1) If the network is opencircuited with the assembly δ' , then either the 1-st or 4-th contact of the i -th block ($i \geq 2$) are opencircuited, or else the 1-st contact of the 1-st block.
- 2) If the network is open-circuited with assembly δ'' , then the 2-nd contact of the i -th block ($i \geq 1$) is open-circuited.
- 3) If the network is short-circuited with the assembly γ' , then either the 3-rd contact of the i -th block ($i \geq 2$) is short circuited or one of the contacts of the 1-st block is short-circuited.
- 4) If the network is short circuited with the assembly γ'' , then either the 1-st or 4-th contacts of the i -th block ($i \geq 2$) are short circuited, or else one of the contacts of the 1-st block. As a result of running through the assemblies T_0 , we obtain one of the possible informations $I_0, I_1, I_2, I_3, I_4, I_5$. These informations are characterized by Table 22.

Each of the informations describes the state of the network, namely: I_0 denotes that either the network is in working order or else there is a short circuit in the 2-nd contact of the i -th block ($i \geq 2$) or an open circuit in the 3-rd contact of the i -th block ($i \geq 2$); I_1 denotes that the open circuit is either in the 1-st or in the 4-th contact of the i -th block ($i \geq 2$), or in the 1-st contact of the 1-st block; I_2 denotes that the open circuit is in the 2-nd contact of the i -th block ($i \geq 1$); I_3 denotes a short circuit in the 1-st block; I_4 denotes a short circuit in the 3-rd contact of the i -th block ($i \geq 2$); I_5 denotes a short circuit either in the 1-st or in the 4-th contact of the i -th block ($i \geq 2$).

Table 22

Assemblies	I_0	I_1	I_2	I_3	I_4	I_5
δ'	1	0	1	1	1	1
δ''	1	1	0	1	1	1
γ'	0	0	0	1	1	0
γ''	0	0	0	1	0	1

Now, to complete the construction of the tentative test, it remains to write out the tests T_{I_i} :

$$T_{I_0} = \{\alpha^2, \alpha^3, \dots, \alpha^n; \beta^2, \beta^3, \dots, \beta^n\},$$

$$T_{I_1} = \{\varepsilon, \alpha^2, \alpha^3, \dots, \alpha^n\},$$

$$T_{I_2} = \{\varepsilon, \alpha^2, \alpha^3, \dots, \alpha^{n-1}\},$$

$$T_{I_3} = N \text{ --- empty set}$$

$$T_{I_4} = \{\beta^1, \beta^2, \dots, \beta^{n-1}\},$$

$$T_{I_5} = \{\beta^1, \beta^2, \dots, \beta^n\}.$$

The fact that the listed sets $T_{I_0}, T_{I_1}, T_{I_2}, T_{I_3}, T_{I_4}, T_{I_5}$ are tests, following directly from the arguments given in Sec. 8.

We note that a tentative test essentially represents a scheme for proving that the set $\{T_0, T_{I_1}, \dots, T_{I_{S_0}}\}$ is a (unconditional) test. This note makes it possible to extract in many cases the construction of the conditional test from the proof of the test.

To describe a conditional test we consider the mathematical expectation of the length $t = t_0 + t_{I_i}$ of the employed portion of the conditional test. This quantity is proportional to the average time of monitoring the network.

The introduced probability characteristic is meaningful if it is established that the faults appear with a definite frequency. In practice one can always consider that this takes place, when we deal with an

adjusted network. In this case one can determine by statistical means the probabilities of the appearance of various faults. We denote by $P(I_i)$ the probability that in running through T_0 we obtain the information I_i . Obviously, the sought mathematical expectation can be found from the formula

$$t = \sum_{i=1}^s (t_0 + t_{I_i}) P(I_i) = t_0 + \sum_{i=1}^s t_{I_i} P(I_i),$$

since

$$\sum_{i=1}^s P(I_i) = 1.$$

We calculate t for the preceding example.

Let p be the probability of the network being in working order, $q = 1 - p$ the probability that there is a single fault in the network -- a short circuit or an open contact.* We assume that the probability of all the faults are equal to each other, i.e., $q/2(4n - 2)$.

We calculate the values of $P(I_i)$

$$P(I_0) = p + \frac{n-1}{4n-2} q, \quad P(I_1) = \frac{2n-1}{2(4n-2)} q = \frac{q}{4}, \quad P(I_2) = \frac{n}{2(4n-2)} q,$$

$$P(I_3) = \frac{q}{4n-2}, \quad P(I_4) = \frac{n-1}{2(4n-2)} q, \quad P(I_5) = \frac{n-1}{4n-2} q;$$

$$t = 4 + \left(p + \frac{n-1}{4n-2} q \right) 2(n-1) + \frac{q}{4} n + \frac{n}{2(4n-2)} q(n-1) + \\ + \frac{n-1}{2(4n-2)} q(n-1) + \frac{n-1}{4n-2} qn = 2n + 2 - q \left[\frac{3}{4} n - \frac{7}{8} - \frac{1}{8(2n-1)} \right].$$

Since $t_y = 2n + 2$, then

$$t = t_y - q \left[\frac{3}{4} n - \frac{7}{8} - \frac{1}{8(2n-1)} \right].$$

* This relation shows that the average length of the tentative test differs substantially from the length of the tentative test in the case when q is not very small. However, if q is not very small, then the network operates with frequent breakdowns and consequently needs adjustment. Thus, under normal conditions the average length of the tentative test deviates little from the length of the tentative test.

* Consequently, the probability of appearance of faults in more than one contact is 0.

In the preceding argument the calculation was based on the assumption that the tests T_{I_i} are run through completely. However, there is no need for running through T_{I_i} completely, if the fault has already been localized. Consequently, it is convenient to consider each of the tests T_{I_i} as an ordered test.

10. Test for a Binary Summator Network

The advantage of the conditional test is particularly clearly seen from an examination of the problem of finding a single fault for a single binary summator network /1/.

We start with the following scheme for adding two n -column numbers, specified in binary form

$$\begin{array}{r} + a_n a_{n-1} \dots a_1 \\ b_n b_{n-1} \dots b_1 \\ \hline s_{n+1} s_n s_{n-1} \dots s_1 \end{array}$$

If we denote by c_i the result of the carry in the $(i + 1)$ -th column, we obtain the following recursion formulas

$$\begin{aligned} s_i &= \bar{a}_i(b_i c_{i-1} \vee b_i \bar{c}_{i-1}) \vee a_i(b_i c_{i-1} \vee b_i \bar{c}_{i-1}), \\ c_i &= \bar{a}_i b_i c_{i-1} \vee a_i(b_i \vee b_i \bar{c}_{i-1}), \\ c_i &= \bar{a}_i(b_i \vee b_i \bar{c}_{i-1}) \vee a_i b_i c_{i-1}, \end{aligned}$$

where $i = 1, 2, \dots, n$, $c_0 = 0$, $s_{n+1} = c_n$.

Starting with these relations, it is easy to obtain the binary summator of interest to us. This network consists of n blocks of three types (Fig. 43).

The blocks are connected as shown in Fig. 44.

Thus, the binary summator network represents a block network. However, unlike the comparison network, we have here a more complicated connection between blocks. It is therefore quite natural to refine further the procedure for setting up tests for the block networks.

Assume (1) that we have a network made up of a small number of types of different blocks. We assume

furthermore (2) that no relay can act on several blocks, and that each block is controlled by a small number of relays. Finally, we assume (3) that in each type of block's the poles are broken up in an identical manner into inputs and outputs so that the inputs (or respectively the outputs) have the separability property (see below, p. 342 of source) and that in the network the current always enters into a block which is in working order only through the inputs and leaves the block only through the outputs.*

* This limitation is imposed in order to facilitate the calculations.

In the investigation of block diagrams we first make up, in accordance with the network, a table of "transfer" and "output" numbers, which shows the dependence of the states of the output on the states of the input in the case when the given block is in working order. This table explains the possible states of the inputs of a given block under the assumption that all the remaining blocks are in working order.

The next stage is to disregard the connections between blocks and to consider each block independently as a multi-terminal network. The state of this

multi-terminal network is determined by specifying an assembly $\alpha_1^i, \dots, \alpha_k^i, \beta_1^i, \dots, \beta_l^i$, where $\alpha_1^i, \dots, \alpha_k^i$ and $\beta_1^i, \dots, \beta_l^i$ describes respectively the state of the inputs and the relays of the given block. Obviously the state of the outputs of the multi-terminal network will determine the value of $F(\alpha_1^i, \dots, \alpha_k^i, \beta_1^i, \dots, \beta_l^i)$ of the function F . Using the general algorithm described in Chap. I, we can construct a minimal test. These assumptions reduce to the fact that we shall deal with a small number of uncomplicated tables of fault functions. The latter leads to a relative simplicity of calculations. The constructed tests for the blocks give the necessary conditions that characterize the test for the entire network: namely they indicate what combinations of significant figures should be encountered in the assemblies belonging to the test. This makes it possible to construct the base of the test, i.e., the set of assemblies containing the maximum number of assemblies and having the following properties.

Let us take an arbitrary block. Corresponding to this block is a group of variables. Each assembly β of the base of the test determines an assembly for the considered block, and for this it is necessary to join to part $\beta_1^i, \dots, \beta_l^i$ of the assembly $\beta =$

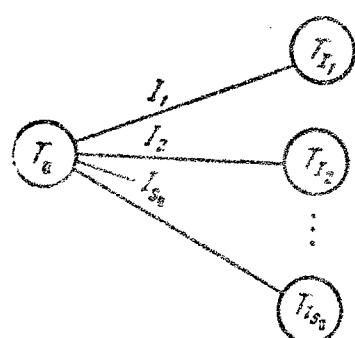


Fig. 41

1-st block

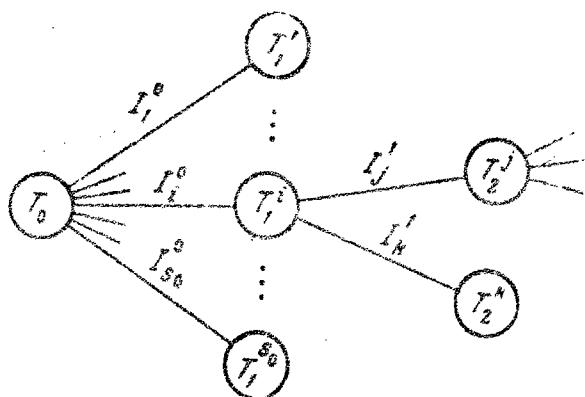
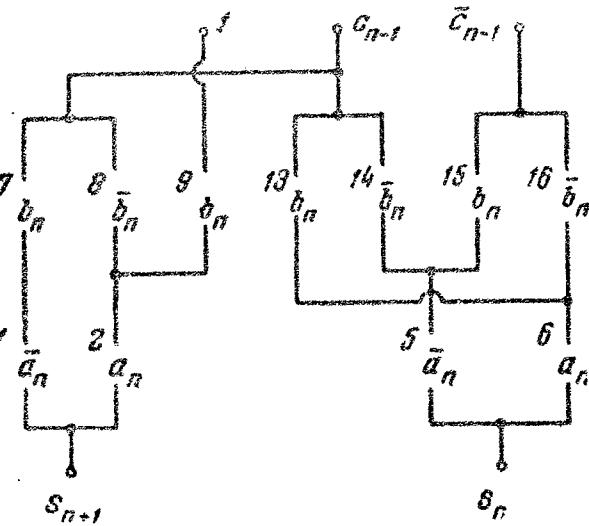
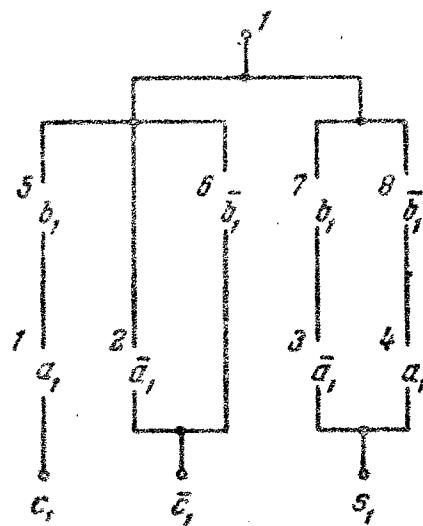


Fig. 42

n-th block



i-th. block $(2 \leq i \leq n-1)$

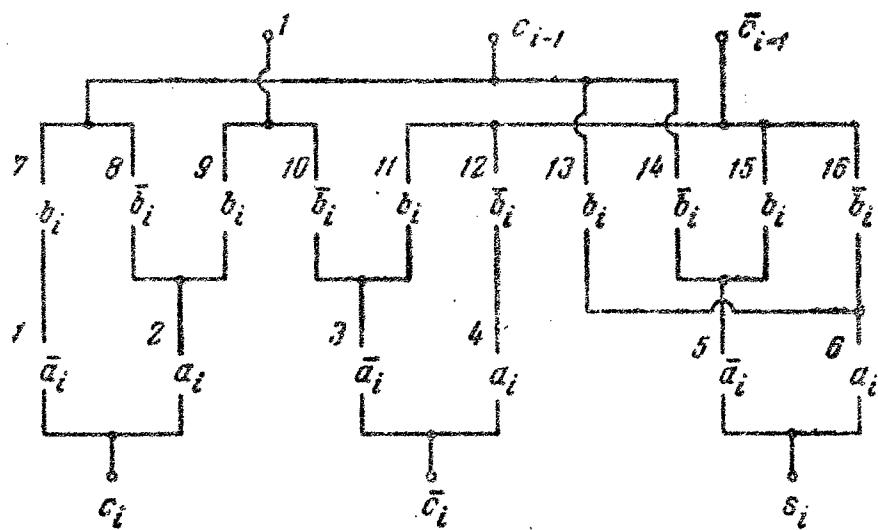


Fig. 43

$\beta = (\dots, \beta_1^i, \dots, \beta_k^i, \dots)$, corresponding to the given variables, the assembly $\alpha_1^i, \dots, \alpha_k^i$, corresponding to the states of the inputs of the considered block, when the network is in the state β . The constructed set of assemblies $\{\alpha_1^i, \dots, \alpha_k^i, \beta_1^i, \dots, \beta_k^i\}$ should be a test for the i -th block.

We shall not give here a formal description of the construction of the base of the test relative to a minimal test of each block. We note only that even if it is known that the i -th block is out of order, we cannot always, generally speaking, determine with the aid of the base of the test the character of the fault (see Sec. 8, item 3), since the state of the network is determined from the states of the inputs of the network, and the state of the i -th block is determined from the states of the outputs of the block. Thus, the base of the test, as a rule, will not be a test and it must be broadened to a test. This step requires a more rigorous accounting of the character of the connections between the blocks.

Let us consider a block network satisfying condition 3. This limitation is stronger than the requirement that the inputs and the outputs of the blocks be separable, i.e., the requirement that the admittances between each pair of inputs (outputs) of

each block be identically equal to 0. (see Reference 18).

In fact, let each block consist of one contact, i.e., let it have one input and one output, and then in the network shown in Fig. 45, each block is trivially separable, but condition (3) is violated for the "bridge" block v (Fig. 45). Thus, condition (3) imposes limitations not only on the properties of the blocks but also on the properties of their connections.

The concept of separability along with other limitations was introduced by Shannon 18 for one special case of the junction of multi-terminal networks, in order to exclude the presence of admittances from one pole to another, which, leaving the block, again would return to it and again leave it (Fig. 46). Incidentally, for block networks satisfying requirement 3, the existence of conducting circuits,* which return to a given block (feedback), as shown, for example, in Fig. 47, is not excluded. The presence of feedback raises difficulties in the investigation of block networks. We shall not attempt to offer a general theory for such networks, but to eliminate "returning" circuits we shall first narrow down the class of admissible block networks. For this purpose we consider networks which represent "series connections" of

blocks, in each of which the poles are broken up into inputs and outputs. When connected in series, the blocks form an ordered aggregate. With this, the network either has a single input and several outputs or a single output and several inputs. In the former case the input of the network can be joined to any input of each block, and the outputs of the network can be connected with the outputs of the blocks; in the second case the output of the network can be connected with any output of each block and the inputs of the network can be connected with the inputs of the blocks.

* By conducting circuit is meant here a circuit between arbitrary vertices of the network, for which the admittance is not equal to 0 identically.

In addition, only connections between the outputs of a block and the inputs of the next block, or between the inputs of a block and the outputs of the preceding block, are possible. For the former case the series connection of the blocks is shown schematically in Fig. 48.

Examples of networks of this type are a network for parity counting, a comparison network, and the binary-summator network.

Let us assume now that there is a fault in the i -th block. Obviously, this fault can change the state of the outputs not only of the i -th block alone. The latter circumstance is due to the fact that as a result of the fault there is a possibility of current flowing along new circuits both on the side of the $(i + 1)$ -th block (forward wave) and on the side of the $(i - 1)$ -th block (backward wave). It is clear that if no limitations are imposed, a wave moving in a definite direction may in a certain block be "reflected" and returned in a backward direction. This phenomenon can take place with multiple reflections. Thus, in networks represented by series connection of blocks, feedback can also exist. The occurrence of reflected waves makes the calculation of the changes in the states of the outputs very difficult. However, in the cases considered here no wave reflection takes place and this allows us to examine independently the changes in the states of the outputs of the $(i + 1)$ -th, $(i + 2)$ -th, ... blocks due to the influence of the forward wave, and changes of the states of the outputs of the $(i - 1)$ -th, $(i - 2)$ -th, ... blocks due to the influence of the backward wave.

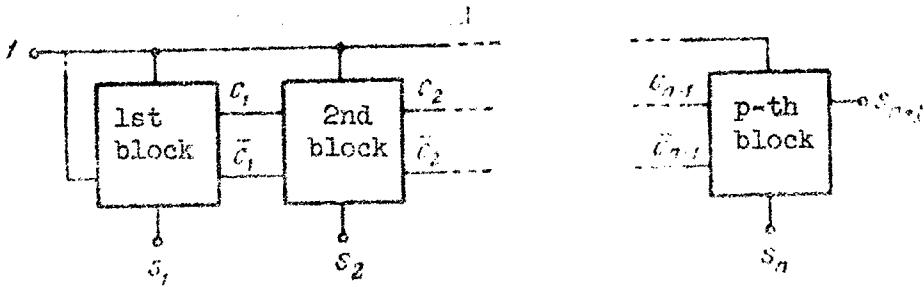


Fig. 44

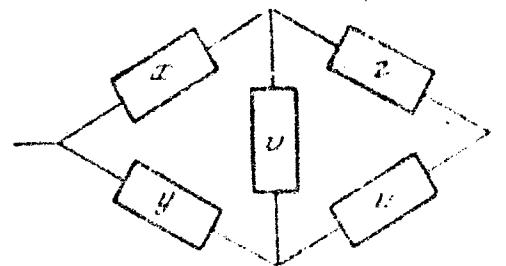


Fig. 45



Fig. 46

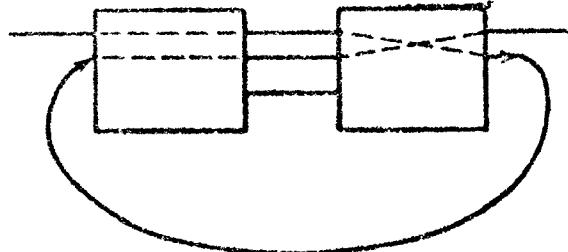


Fig. 47

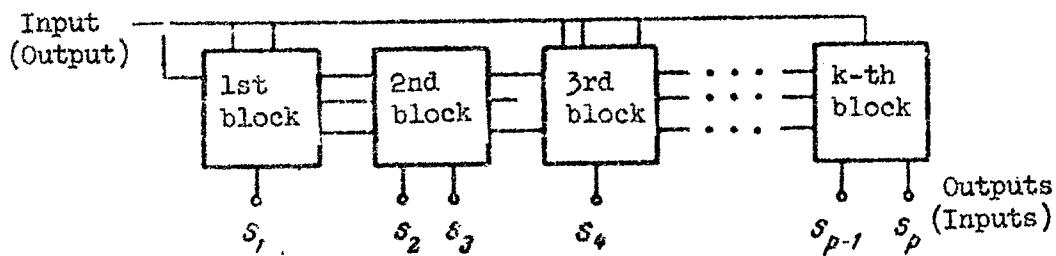


Fig. 48

Table 23

$c_{i-1}c_{i+1}$	0 0	0 1	1 0	1 1
a_ib_i	$c_ic_is_i$	$c_ic_is_i$	$c_ic_is_i$	$c_ic_is_i$
0 0	0 1 0	0 1 0	0 1 1	0 1 1
0 1	0 0 0	0 1 1	1 0 0	1 1 1
1 0	0 0 0	0 1 1	1 0 0	1 1 1
1 1	1 0 0	1 0 0	1 0 1	1 0 1

Table 24
(1st half)

Table of Fault Functions

		Short															
Carry	a_i	b_i	0	1	2	3	4	5	6	7	8	9	10	11	12	13	14
0	0	0	2						3		3					3	
	0	1	3	7				7		7						7	
	1	0	3				7			7						7	
	1	1	4	5	6	5			5						6		5
	0	0	3	7				7									
	0	1	4					7			7					7	
1	0	1	4											7			
	1	0	4		7	7							7		7		
	1	1	5														

fault in 1-th block ($2 \leq i \leq n$)

Table 24

Table 24
(2nd half)

		Break												N ₀ W/41						
		15	16	1'	2'	3'	4'	5'	6'	7'	8'	9'	10'	11'	12'	13'	14'	15'	16'	
3																				1
7																				2
7																				3
5																				4
5	0																			5
7																				6
7	0																			7
																				8

Table 25

Table of Fault Functions in 1st Block a

a_1	b_1	Short						Break			N_2 n.u
		1	2	3	4	5	1'	2'	3'	4'	
0	0	2		3							1
0	1	3	7				1	2			2
1	0	3				7			2	1	3
1	1	4		6	5		0				4

We shall consider below exclusively only those networks that satisfy conditions (1) -- (3) and represent a series-connected blocks. The following theorem gives a criterion for the absence of reflected waves.

Theorem. There are no reflected waves if a network, representing a series connection of blocks and having properties (3) contains a single fault.

The proof is almost obvious.

Note. In networks representing a series connection of blocks, the presence of property (3) is equivalent to the presence of separability of the inputs and outputs of each block and to the forbiddenness of the connection between one output (input) of a block and several inputs (outputs).

We shall see later on that by tracing the waves one can choose the base for a test and then broaden it to a test having sufficiently short length.

We now show the appearance of the construction of a conditional test for a binary summator.

Since the foregoing theorem holds for a binary-summator network, we are justified in considering the effect of the waves independently. We first investigate the effect of the forward wave. Since the construction of the test for a binary summator is cumbersome, we shall break down this process into stages.

I. Compilation of a Table of Transfer and Output Numbers. In order to take into account the connections between blocks and also in order to clarify the permissible states of the outputs of the faulty block, we make up a table (see Table 23) of transfer and output numbers for the i -th block ($2 \leq i \leq n - 1$). It is easily seen that the outputs of the faulty block can be only in one of two possible states, (0 1) and (1 0). We shall use this circumstance in the next step.

II. Compilation of Tables of Fault Functions. Here we start with numbering the contacts as indicated in the diagrams. In the diagram of the n -th block we use a non-through numbering, since this reflects the fact that the n -th block is obtained from the i -th block ($2 \leq i \leq n - 1$) by excluding a series of contacts, connected with the output \bar{c} . In the fault tables 24 -- 26, the states of the inputs are written in the form of two-digit binary numbers; the states of the outputs are written for the sake of brevity as decimal numbers corresponding to the binary numbers $c_i \bar{c}_i s_i$ ($i = 1, 2, \dots, n - 1$) and $s_{n+1} \dots s_n$. From Table 24 we have $f_0 = f_4$, $f_{13} = f_{15}$, $f_{14} = f_{16}$, $f_{11} = f_{71}$, and $f_{14} = f_{12}$. From the diagram of the 1-st block (see Fig. 43) it is seen that $f_2 = f_6$, $f_3 = f_8$, $f_4 = f_7$,

$f_1^* = f_5^*$, $f_3^* = f_7^*$, and $f_4^* = f_8^*$.

By virtue of the symbols used, and also by virtue of the structure of the n -th block, the table of fault functions for the n -th block (Table 26) is obtained from the table of fault functions for the i -th block (Table 24) by leaving in the latter the corresponding columns and replacing them 2 by 0, 3 by 1, 6 by 4, and 7 by 6 (the second binary digit is always 0). From Table 26 we have

$f_{13} = f_{15}$, $f_{14} = f_{16}$, and $f_{1*} = f_{7*}$.

From the foregoing tables 24 -- 26 it is seen that certain faults have become indistinguishable. The question arises: ... what can be said relative to the indistinguishability of faults in the entire network? Thus, let f_j^i denote a function of the j -th fault of the i -th block, f_0 -- a function corresponding to the operation of the properly-working network.* Since in the network under consideration there is no feedback (reflection of waves) and since no feedback appears for faults of the open-circuit type, it is obvious that we have for the 1-st block

$$f_1^1 = f_0, f_3^1 = f_0, f_4^1 = f_0,$$

for the i -th block ($2 \leq i \leq n - 1$)

$$f_1^i = f_0, f_4^i = f_0,$$

and for the n -th block

$$f_1^* = f_7^*$$

* Here the functions depend on $2n$ arguments $\begin{pmatrix} a_1, \dots, a_n \\ b_1, \dots, b_n \end{pmatrix}$, which assume values 0 and 1; the values of the functions themselves are integers from the segment $[0, 2^{n+2} - 1]$.

Furthermore, since all the circuits that arise as the result of feedback and go to the output s_1 of the 1-st block pass through the input of the network, these feedbacks provide no new possibilities for monitoring either the 1-st or the 2-nd block. Therefore

$$f_2^* = f_6^*, f_3^* = f_8^*, f_4^* = f_7^*$$

$$f_9^* = f_4^*, f_{10}^* = f_{15}^*, f_{11}^* = f_{16}^*$$

It is seen therefore that the 4-th contact of the 2-nd block is superfluous.

We shall show below that $f_{13}^i = f_{15}^i$ and $f_{14}^i = f_{16}^i$ when $3 \leq i \leq n$, and also that no new identifications are produced (all the remaining faults will differ).

It is easy to establish from Tables 24 -- 26 that assemblies 1 -- 4 are a minimal test (trivial) for the verification of the 1-st block, and that

L

Table of Fault Functions in n-th Block

		Short																
		a_n	b_n	0	1	2	3	4	5	6	7	8	9	10	11	12	13	14
0 1	0	0	0							1					1	1		
	0	1	1							5					5			
	1	0	1							5					5	5		
	1	1	4							5					5			
	0	0	1							5					5			
	0	1	4							5					5			
1 0	1	0	4							5					5			
	1	1	5															
	0	0	1							5					5			

Table 26
(2nd half)

		Break									N ₄				
		15	16	1'	2'	5'	6'	7'	8'	9'	13'	14'	15'	16'	n. n
1															1
5															2
5															0
5															0
5															3
5															4
5															5
5															6
5															7
5															8

Assemblies 2--8 are a minimal test for the verification of the i -th block ($2 \leq i \leq n$). In fact, the direct breakdown (see Chapter I, Sec. 3) shows that the foregoing sets are tests. Since assemblies 1 -- 4 in the case of the 1-st block and assemblies 2 -- 8 in the case of the i -th block ($i \geq 2$) must enter (Chap. I, Sec. 3, Item 3) into any test for the corresponding block, the foregoing sets are minimal tests.

III. Construction of T_0 -- The Base of the Test.

Now, starting out with tests for the individual blocks and a table of transfer numbers, we shall attempt to construct assemblies that form the set T_0 in such a way, that T_0 have the least possible length and that the information obtained after running through T_0 would permit ready implementation of the conditional test by adding in each individual case a small number of assemblies.

Inasmuch as in the investigated network the 1-st block occupies a special position, we shall ^{not} _A take into account the test for the 1-st block in the construction of T_0 . Thus, we shall construct such a set T_0 that for any i ($2 \leq i \leq n$) the set of assemblies, each of which is $c_{i-1} \bar{c}_{i-1} \alpha_i \beta_i$, where c_{i-1} is the result of carry in the i -th column, and α_i and β_i are the i -th columns of the numbers of the set from T_0 , forms a test for the i -th block. Obviously, this construction can

lead to several different versions of T_0 . We take for T_0 the set $\{e_1, e_2, e_3, e_4, e_5, e_6, e_7\}$, where

$$e_1 = \begin{pmatrix} 0 & \dots & 0 & 0 \\ 1 & \dots & 1 & 1 \\ 0 & \dots & 0 & 0 \\ 1 & \dots & 1 & 1 \end{pmatrix}, \quad e_2 = \begin{pmatrix} 1 & \dots & 1 & 1 \\ 0 & \dots & 0 & 0 \\ 0 & \dots & 0 & 0 \\ 1 & \dots & 1 & 1 \end{pmatrix}, \quad e_3 = \begin{pmatrix} \dots & 0 & 1 & 0 & 1 \\ \dots & 0 & 1 & 0 & 1 \end{pmatrix}, \quad e_4 = \begin{pmatrix} \dots & 1 & 0 & 1 & 0 \\ \dots & 1 & 0 & 1 & 0 \end{pmatrix},$$

$$e_5 = \begin{pmatrix} 0 & \dots & 0 & 1 \\ 1 & \dots & 1 & 1 \\ 0 & \dots & 0 & 1 \\ 1 & \dots & 1 & 1 \end{pmatrix}, \quad e_6 = \begin{pmatrix} 1 & \dots & 1 & 1 \\ 0 & \dots & 0 & 1 \\ 1 & \dots & 1 & 1 \end{pmatrix}, \quad e_7 = \begin{pmatrix} 1 & \dots & 1 & 1 \\ 1 & \dots & 1 & 1 \end{pmatrix}.$$

The assemblies of the set T_0 are connected with the assemblies of the minimal test for the i -th block as follows: the assembly e_1 is constructed starting with assemblies 2, e_2 is constructed starting with assemblies 3, e_3 -- starting with assemblies 4, 5, e_4 -- starting with assemblies 4, 5, e_5 -- starting with assemblies 6, e_6 -- assemblies 7, and e_7 -- assemblies 8.

It should be noted here that the length t of any unconditional test T (and also of the base of the test) is not less than 7 when $n \geq 2$, i.e., $t \geq 7$.

To prove this statement we must establish that allowance for the feedbacks cannot reduce the test for the n -th block.

Since in the case of an open circuit no feedbacks are produced, if they do not exist in the original network, assemblies 2, 3, 5, 6, 7, and 8 must enter into any test (see Table 26). It is obvious that the closing of the first contact can be detected only when $a_n = b_n = 1$

(see diagram, Fig. 43); here the feedback is produced when there is no carry from the preceding block, i.e., $c_{n-1} = 0$. However, under these conditions closing in the 1-st block is caught directly by the presence of a 1 at the output s_n .

Thus, any test must contain the assembly (0 1 1 1), i.e., assembly 4. This proves the statement.

IV. Compilation of Information Tables. As a result of running through the assembly e_j we obtain a $(n + 1)$ -column assembly. Let us write out the result of running through assemblies e_1, e_2, \dots, e_7 under the assumption that there is a given fault in the i -th block ($i \geq 2$) and in the 1-st block. In Tables 27 -- 29 we shall show only those results which differ from the correct values.

Table 27

Assemblies of base	0	Short in i-th block											
		1	2	3	4	5	6	7	8	9	10	11	12
		q	u	v	w	q	u	v	w	q	u	v	w
e_1	01 . . . 1		2	2			2	2			2	2	2
e_2	01 . . . 1				2	2			2			2	
e_3	• . . 1010	3	3	3	3	3	3	3	3	3	3	3	3
e_4	• . . 0101	3	3	3	3	3	3	3	3	3	3	3	3
e_5	10 . . . 00					2			2		2	2	2
e_6	10 . . . 00			2		2			2		2		
e_7	11 . . . 10												
Types of Info.		I_0	I_1	I_2	I_3	I_4	I_5	I_6	I_7	I_8	I_9	I_{10}	I_{11}

Table 28

Assem- blies of base	Short in i -th Block											
	2'		3'		4'		5'		6'		7'	
	odd	even	odd	even	odd	even	odd	even	odd	even	odd	even
e_1					e_4	η_4						
e_2					e_5		η_5					
e_3					θ_4		θ_5					
e_4							λ_4					
e_5	μ							μ				
e_6		μ		μ					μ			
e_7		ν_{4+1}		ν_{4+1}				ν_5		ν_{6+1}		ν_{6+1}
Types of Info.	I_{14}	I_{15}	I_{16}	I_{17}	I_{18}	I_{19}	I_{20}	I_{21}	$I_{14} I_{22}$	I_{23}	I_{24}	$I_6 I_{17} I_{18} I_{25} I_{26} I_{27} I_{28} I_{29}$

Table 29

Table 29

Assemblies or base	Short in 1st block								Break in 1st block							
	1	2	3	4	5	6	7	8	1'	2'	3'	4'	5'	6'	7'	8'
e_1	α								ϵ_1	η_1						
e_2											η_1					
e_3									β_1	β_1	β_1	β_1	β_1	β_1	β_1	β_1
e_4										γ_1						
e_5																λ_1
e_6																
e_7																
Types of info.	I_{30}	I_{31}	I_{32}	I_0	I_{33}	I_{31}	I_0	I_{32}	I_{34}	I_{35}	I_{36}	I_{37}	I_{38}	I_{36}	I_{37}	

The plain numbers and the primed numbers in Tables 27 -- 29 denote closing and opening, respectively, of a contact designated by this number; 0 denotes, as always, the network in working order. Certain columns are split, depending on whether the number i is even (e) or odd (o). When $i = n$ the columns in Tables 27 and 28, corresponding to the indices 3, 4, 10, 11, and 12, need not be considered. After these explanations, let us write out the values of the following parameters which enter into Tables 27 -- 29:

$$\begin{aligned} a &= 11 \dots 11, \delta = 11 \dots 10, \\ \mu &= 00 \dots 00, \alpha = 10 \dots 01. \end{aligned}$$

The remaining parameters are given in Table 30.

A survey of Tables 27 -- 29 shows that we have 39 different types of information. We shall not write out a table of information in explicit form, and shall confine ourselves only to an indication, at the end of each column, of the information with which a given fault is connected.

As a result of running through the base we obtain quite definite information, which contains not only the type of information, but also as a rule the value of the index i for the parameters $\beta_i, \gamma_i, \varepsilon_i, \eta_i, \nu_i, \vartheta_i$, and λ_i . Let us write now a list of faults, connected

Table 30

	$n+1$	i	21	
β_1	0	010111	10	For i even
β_2	0	01011	10	For i odd
γ_1	0	01011	01	For i even
γ_2	0	010111	01	For i odd
η_1	0	001	11	
η_2	01	110	11	
η_3	0	010100	10	For i even
η_4	0	101000	10	For i odd
λ_1	0	101000	01	For i even
λ_2	0	010100	01	For i odd
γ_4	1	110	10	

Note: It is obvious that $\beta_{2k+1} = \beta_{2k}$, $\gamma_{2k-1} = \gamma_{2k}$, $\eta_{2k+1} = \eta_{2k}$, $\lambda_{2k+1} = \lambda_{2k}$.

with given information. We shall distinguish here two cases.

a) The information determines uniquely faults, the indistinguishability of which is established.

I_6 -- presence of a short circuit in the 5-th contact of the i -th block, i.e. 5_i

where i -- even,

I_7 -- " " " " " 5-th contact of the i -th block, i.e. 5_i

where i -- odd,

I_{15} -- " " an open circuit in the 2nd contact of the i -th block, i.e. 2_i

where i -- even,

I_{16} -- " " " " " " 2nd contact of the i -th block, i.e. $2'_i$

where i -- odd

I_{18} -- " " " " " " 4-th or 12-th contact of the i -th block, i.e., 4_i

$\vee 12'_i$,

I_{19} -- " " " " " " 5-th contact of the i -th block, i.e. $5'_i$, where i -- even

I_{20} -- presence of an open circuit in the 5-th contact,
i.e., $5_i^!$, where
 i -- odd

I_{21} -- " " " " " " 6-th contact,
i.e., $6_i^!$,

I_{23} -- " " " " " " 9-th contact,
i.e., $9_i^!$, where
 i -- even,

I_{24} -- " " " " " " 9th contact,
i.e., $9_i^!$, where
 i -- odd

I_{25} -- " " " " " " 13-th contact,
i.e., $13_i^!$,

I_{26} -- " " " " " " 14-th contact,
i.e. $14_i^!$, where
 i -- even

I_{27} -- " " " " " " 14-th contact,
i.e. $14_i^!$, where
 i -- odd

I_{28} -- " " " " " " 15-th contact,
i.e. $15_i^!$, where
 i -- even

I_{29} -- " " " " " " 15-th contact,
i.e. $15_i^!$, where
 i -- odd

I_{30} -- presence of shortcircuit in the 1-st contact of the
 1-st block, i.e. 1_1
 I_{31} -- " " " " " " 2-nd or 6-th contact
 of the 1-st block,
 i.e. $2_1 \vee 6_1$
 I_{32} -- " " " " " " 3-rd or 8-th contact
 of the 1-st block,
 i.e. $3_1 \vee 8_1$
 I_{33} -- " " " " " " 5-th contact of the
 1-st block, i.e. 5_1
 I_{34} -- " " open " " " 1-st and 5-th contacts
 of the 1-st block,
 i.e. $1'_1 \vee 5'_1$
 I_{35} -- " " " " " " 2-nd contact of the
 1-st block, i.e. $2'_1$
 I_{36} -- " " " " " " 3-rd or 7-th contacts
 of the 1-st block,
 i.e. $3'_1 \vee 7'_1$
 I_{37} -- " " " " " " 4-th or 8-th contacts
 of the 1-st block,
 i.e. $4'_1 \vee 8'_1$
 I_{38} -- " " " " " " 6-th contact of the
 1-st block, i.e. $6'_1$

b) The information determines directly several
 faults, which are either distinguishable, or those

for which the distinguishability has not been established for certain values of i .

I_0 -- denotes that either the network is in working order, or there is a short circuit in the 4-th or 12-th contacts of an unknown block or in the 4-th or 7-th contact of the 1-st block, or else the presence of an open circuit in the 10-th contact of an unknown block, i.e., $0 \vee 4 \vee 12 \vee 4_1 \vee 7_1 \vee 10'$;

I_1 denotes the presence of a short circuit in the 1-st contact of the i -th block, or in the 7-th contact of the $(i - 1)$ -th block, i.e., $1_i \vee 7_{i-1}$, where i is even ($2 \leq i \leq n + 1$);

I_2 denotes the presence of a short circuit in the 1-st contact of the i -th block or in the 7-th contact of the $(i - 1)$ -th block, i.e., $1_i \vee 7_{i-1}$, where i is odd ($2 \leq i \leq n + 1$);

I_3 denotes a presence of a short circuit in the 2-nd contact of the i -th block or in the 8-th contact of the $(i + 1)$ -th block, i.e., $2_i \vee 8_{i+1}$, where i is even ($1 \leq i \leq n$);

I_4 denotes the presence of a short circuit in the 2-nd contact of the i -th block or in the 8-th contact of the $(i + 1)$ -th block, i.e., $2_i \vee 8_{i+1}$, where i is odd ($1 \leq i \leq n$);

I_5 denotes the presence of a short circuit in the

3-rd or 11-th contact of an unknown block, i.e., $3 \vee 11$;

I_8 denotes the presence of a short circuit in the 6-th contact of an unknown block, i.e., 6;

I_9 -- denotes the presence of a short circuit in the 9-th contact of an unknown block, i.e., 9;

I_{10} -- denotes the presence of an open circuit in the 10-th contact of an unknown block, i.e., 10;

I_{11} -- denotes the presence of a short circuit in the 13-th or 15-th contacts of an unknown block, i.e., $13 \vee 15$;

I_{12} -- denotes the presence of a short circuit in the 14-th or 16-th contacts of the i -th block, i.e., $14_i \vee 16_i$, where i is even;

I_{13} -- denotes the presence of short circuit in the 14-th or 16-th contacts of the i -th block, i.e., $14_i \vee 16_i$, where i is odd;

I_{14} -- denotes the presence of an open circuit in the 1-st or 7-th contacts of an unknown block, i.e., $1' \vee 7'$;

I_{17} -- denotes the presence of an open circuit in the 3-rd or 11-th contacts of the i -th block, i.e., $3'_i \vee 11'_i$;

I_{22} -- denotes the presence of an open circuit in the 8-th contact of an unknown block, i.e., 8'.

Note. In I_1, I_2, I_3 , and I_4 the faults $7_1, 1_{n+1}, 8_{n+1}$, and 2_1 are fictitious and should be discarded.

The foregoing list shows that in the case of appearance of information indicated in item "a" the fault is established and the monitoring is completed. However, in the appearance of information indicated in item "b" additional analysis is necessary. Since this analysis uses essentially the effect of the backward wave, we shall proceed to consider the backward wave.

V. Effect of the Backward Wave. We have already taken into account in certain auxiliary arguments, considerations that take into account the effect of feedback. Now, on the basis of an account of the effect of the backward wave, we shall, on the one hand, establish the indistinguishability of certain faults, and on the other hand we shall show for certain cases how faults can be detected.

1) Proof that $f_{13}^i = f_{15}^i$ and $f_{14}^i = f_{16}^i$ ($i \geq 2$).

It follows from the table of fault functions that it is impossible to distinguish f_{13}^i from f_{15}^i and f_{14}^i from f_{16}^i if only the effect of the forward wave is taken into account. It remains for us to show that this is also impossible if the action of the backward wave is considered. In fact, for any assembly e , both in the

case of closing of the contact 13 and in the case of the closing of the contact 15 (or respectively the closing of contacts 14 and 16), either the outputs of the $(i - 1)$ -th block are simultaneously closed, and then in both cases the same backward wave is produced, or else they are simultaneously open and there is no backward wave at all, i.e., $f_{13}^i(e) = f_{15}^i(e)$ (or respectively $f_{14}^i(e) = f_{16}^i(e)$). This proves the statement. It follows therefore that upon appearance of information I_{12} or I_{13} , the analysis of the fault is complete.

2) Proof of Distinguishability of f_4^i from f_0 and f_{12}^i when $i > 2$ (when $i = 2$ we have $f_4^2 = f_0$, see p. 347 /of source/). We agree furthermore to place in the assembly $\begin{pmatrix} a_1 & \dots & \overset{\dagger}{a}_i & \dots & a_j \\ b_1 & \dots & b_i & \dots & b_j \end{pmatrix}$ a "+" or "-" sign above the corresponding column, if we wish to note whether carry ~~took-place-in~~ from the preceding columns took place or not.

Obviously, to detect a short circuit in the 4-th contact of the i -th block by means of the backward wave it is necessary that the verifying assembly contain

$\begin{smallmatrix} 0 \\ 0 \end{smallmatrix}$ in the i -th column (the + guarantees that $\bar{c}_{i-1} = 0$). Furthermore, to observe the appearance of a backward wave on the pole \bar{c}_{i-1} , it is necessary that the $(i - 1)$ -th column of this assembly be $\begin{smallmatrix} \dagger \\ \alpha \end{smallmatrix}$, for then when the 4-th contact of the i -th block is closed we have

$s_{i-1} = 1$ (normally, $s_{i-1} = 0$). Thus, the verifying assembly should have, in the simplest case, the form

$(\dots \begin{smallmatrix} 0 & 0 & 1 \\ 0 & 1 & 1 \end{smallmatrix} \dots)$. Let us ascertain now the result that should be produced here by a carry in the $(i - 2)$ -th column. If $i - 2 > 1$, then the $(i - 2)$ -th block contains the 12-th contact.

Obviously, in the absence of carry in the $(i - 2)$ -th column and upon closing of the 12-th contact of the $(i - 2)$ -th block, we shall have $\bar{c}_{i-2} = 1$ and therefore $s_{i-1} = 0$. Thus, in the absence of carry in the $(i-2)$ -th column ($i > 3$) we shall have $f_4^i \equiv f_{12}^{i-2}$. Consequently, to avoid this identification, it is necessary that when $i > 3$ the investigated assembly have the form

$(\dots \begin{smallmatrix} 0 & 0 & 0 \\ 0 & 1 & 1 \end{smallmatrix} \dots)$. It is seen therefore, that a fault in the 4-th contact of the $i \geq 3$ block (unknown) is determined with the aid of four assemblies, for example:

$(\dots 0 0 1 1 0 0 1 1)$, $(\dots 0 0 1 1 0 0 1)$, $(\dots 0 0 1 1 0 0)$, $(\dots 0 0 1 1 0)$,
 $(\dots 0 1 1 1 0 1 1 1)$, $(\dots 0 1 1 1 0 1 1)$, $(\dots 0 1 1 1 0 1)$, $(\dots 0 1 1 1 0)$.

The remaining faults $0, 4_1 \vee 7_1, 1_i, 2_i, 3_i, 6_i, 7_i, 8_i, 9_i, 10_i, 11_i, 12_i, 13_i \vee 15_i, 1_i^!, 3_i^!, 7_i^!, 8_i^!, 10_i^!,$ and $11_i^!$ can be established in principle by taking into account only the forward wave. However, we shall see later that by using the effect of the backward wave we can construct a more compact conditional test.

VI. Construction of the Tests T_{I_i} . In the case of appearance of information I_1 or I_2 , the index i and the faults $l_i \vee 7_{i-1}$ are determined. To distinguish them, we take the test

$$T_{l_i} = \{e_8\} \text{ or } T_{l_i} = \{e_9\},$$

where

$$e_8 = \begin{pmatrix} 0 \dots 0 & 1^* & 0 \dots 0 \end{pmatrix}^*,$$

Obviously, on running through the assembly e_8 , we have the following:

$$\text{in the case } l_i = 0 \dots 0 1 1^* 0 \dots 0$$

$$\text{in the case } 7_{i-1} = 0 \dots 0 1 0^* 0 \dots 0$$

* The asterisk denotes here the i -th column.

In the case of appearance of information I_3 or I_4 , we also determine the index i and the faults $2_i \vee 8_{i+1}$. To distinguish them, we take the test

$$T_{l_i} = \{e_9\} \text{ or } T_{l_i} = \{e_8\},$$

where

$$e_8 = \begin{pmatrix} 0 \dots 0 & 1 & 0^* & \dots & 0 \end{pmatrix}.$$

Here, upon running through the assembly e_9 , we have the following:

in the case $2_i = 0 \dots 0 1 0 0^* \dots 0$

in the case $8_{i+1} = 0 \dots 0 1 1 0^* \dots 0$

We note that when $i = n$ the information $I_3 (I_4)$ yields 2_n and no further analysis is necessary.

Let us consider the case of appearance of information I_8 , I_9 , and I_{11} . We put

$$T_{I_8} = T_{I_9} = T_{I_{11}} = \{e_{10}\},$$

where

$$e_{10} = \begin{pmatrix} 0 & \dots & 0 \\ 0 & \dots & 0 \end{pmatrix}.$$

In the case of appearance of "1" in the i -th column upon running through the assembly e_{10} , i.e., if $0 \dots 0 1^* 0 \dots 0$ appears, we have respectively 6_i , 9_i , and $13_i \vee 15_i$.

In the case of appearance of the information I_{10} , as seen from the table of fault functions of the i -th block, we must put

$$T_{I_{10}} = \{e_{11}, e_{12}\},$$

where

$$e_{11} = \begin{pmatrix} \dots & 0 & 1 & 0 & 1 \\ \dots & 1 & 1 & 1 & 1 \end{pmatrix}, \quad e_{12} = \begin{pmatrix} \dots & 1 & 0 & 1 & 0 \\ \dots & 1 & 1 & 1 & 1 \end{pmatrix}.$$

Upon running through assemblies $(\dots 1 0^* 1 \dots)$ and $(\dots 0 1^* 0 \dots)$ when the 10-th contact of the i -th block is closed, we have respectively $\dots 1 0 1 1^* 1 0 \dots$

and ... 1 0 1* 1 1 0 ... instead of ... 1 0 1 0* 1 0 ...
 and ... 1 0 1* 0 1 0 ..., i.e., a "1" appears in the
 i-th and (i - 1)-th columns (when $i = 2$, the "1" appears
 only in the first assembly, since the backward wave from
 the second block is not caught). It is seen therefore
 that the number of the faulty block is established.

From the table of the fault functions of
 the i-th block it is also seen that upon appearance of
 information I_{14} it is necessary to take the test

$$T_{I_{14}} = \{e_{11}, e_{12}\}.$$

In fact, the presence of a fault $1_i^! \vee 7_i^!$ is character-
 ized by the fact that in running through the assembly
 $(\dots 0 1 0^* 1 \dots)$ one obtains instead of ... 0 1 0* 1 ...
 the result ... 0 0 0* 1 ... (the "1" of the (i + 1)-th
 column disappears).

In the case of appearance of information I_{17} ,
 one must take the test

$$T_{I_{17}} = \{e_{13}\},$$

where

$$e_{13} = (\dots 0 0 0^* 0 \dots 0 \dots 0).$$

In the case of a fault $3_i^!$, instead of
 ... 0 1 0* 0 ... there appears ... 0 0 0* 0 ... (the
 "1" disappears from the (i + 1)-th column).

Analogously, in the case of appearance of information I_{22} the test $T_{I_{22}}$ is determined for the establishment of the number of the block in which the contact 8 is open circuited. Namely

$$T_{I_{22}} = \{e_{14}, e_{15}\},$$

where

$$e_{14} = \begin{pmatrix} \dots & 1 & 1 & 1 & 1 \\ \dots & 0 & 1 & 0 & 1 \end{pmatrix}, \quad e_{15} = \begin{pmatrix} \dots & 1 & 1 & 1 & 1 \\ \dots & 1 & 0 & 1 & 0 \end{pmatrix}.$$

Here, when the 8-th contact of the i -th block is open circuited, upon running through the assembly

$\begin{pmatrix} \dots & 1 & 1 & 1 & 1 \\ \dots & 0 & 1 & 0 & 1 \end{pmatrix}$ instead of $\dots 1 0^* 1 \dots$ one obtains $\dots 0 0^* 1 \dots$ (the "1" disappears in the $(i + 1)$ -th column).

The informations I_0 and I_5 lead to more complicated explanations and constructions.

Thus, assume that we have the information I_0 . This means that the network can be in one of the states $0 \vee 4 \vee 12 \vee 4_1 \vee 7_1 \vee 10^*$. As already noted, in step V, the verifying assembly for disclosing a short circuit in the 4-th contact of the i -th block ($i > 2$) should contain the following values, in the i -th, $(i - 1)$ -th, and $(i - 2)$ -th columns. In this case upon closing of the 4-th contact of the i -th block, running through the verifying assembly, we

obtain ... 1* 1 1 ..., i.e., there appears a "1" in the $(i - 1)$ -th column. On the other hand, the presence of a carry in the $(i - 2)$ -th column prevents the possibility of the appearance of a "1" in the $(i - 1)$ -th column, because of a short circuit in the 12-th contact of the $(i - 2)$ -th block. Thus, the "1" appearing in the $(i - 1)$ -th column as a result of running through the verifying test of the indicated type is evidence of the presence of a short circuit in the 4-th contact of the i -th block.

To detect a short circuit in 12-th contact of the i -th block it is necessary that the verifying assembly (see table of fault functions and the diagram of the i -th block) have the form $(\dots 0 \overset{0}{T^*} \dots)$. As a result of running through this assembly we obtain in the case of a short circuit of the 12-th contact of the i -th block ... 1 0* ..., i.e., a "1" appears in the $(i + 1)$ -th column.

However, the "1" can appear in the $(i + 1)$ -th column because of the backward wave due to a fault in the 4-th contact of the $(i + 2)$ -th block, i.e., if the assembly has the form $(\dots 0 \overset{0}{0} T^* \dots)$. To block the path of the backward wave in the $(i + 1)$ -th block, it is enough to take the assembly $(\dots 1 0 T^* \dots)$.

It is easy to see that now the "1" will appear in the $(i + 1)$ -th column upon running through the assembly only if there is a short circuit in the 12-th contact of the i -th block. Finally, to observe an open circuit in the 10-th contact of the i -th block it is necessary to take the assembly $(\dots 0 \ 0^* \ \dots \ 1 \ 0 \ \dots)$ (see table of fault functions and the diagram of the i -th block). It is easy to verify that if upon running through this assembly we obtain $\dots 0 \ a^* \ \dots$, i.e., if the "1" has disappeared from the $(i + 1)$ -th column, then the 10-th contact of the i -th block has become open circuited.

Let us show that in the case of appearance of information I_0 , the completion of the monitoring calls for taking the test

$$T_{I_0} = \{e_{16}, e_{17}, e_{18}, e_{19}, e_{20}, e_{21}\},$$

where

$$e_{16} = (\dots 1 \ 0 \ 1 \ 0 \ 0 \ 0 \ 1 \ 0 \ 1),$$

$$e_{17} = (\dots 0 \ 1 \ 0 \ 0 \ 0 \ 1 \ 0 \ 1 \ 0),$$

$$e_{18} = (\dots 1 \ 0 \ 0 \ 0 \ 1 \ 0 \ 1 \ 0 \ 0),$$

$$e_{19} = (\dots 0 \ 0 \ 0 \ 1 \ 0 \ 1 \ 0 \ 0 \ 1),$$

$$e_{20} = (\dots 0 \ 0 \ 1 \ 0 \ 1 \ 0 \ 0 \ 0 \ 1),$$

$$e_{21} = (\dots 0 \ 1 \ 0 \ 1 \ 0 \ 0 \ 0 \ 1 \ 1).$$

The foregoing assemblies are based on the repetition of the combination $(\begin{smallmatrix} 0 & 0 & 0 & 1 & 0 & 1 \\ 1 & 0 & 1 & 1 & 1 & 1 \end{smallmatrix})$. In assemblies e_{19} and e_{21} we took for the 1-st column $\begin{smallmatrix} 1 \\ 1 \end{smallmatrix}$ and not $\begin{smallmatrix} 0 \\ 1 \end{smallmatrix}$, to ensure transfer to the next column.

If upon running through the assembly e_{18} a "1" appears in the 1-st column, we obviously have $\begin{smallmatrix} 4 \\ 1 \end{smallmatrix} \vee \begin{smallmatrix} 7 \\ 1 \end{smallmatrix}$. If the network is in proper working order, running through any of the foregoing assemblies leads to an assembly in which pieces 0 0, 0 1, and 1 1 alternate (from right to left), where 0 0 is followed by 0 1, 0 1 is followed by 1 1, 1 1 by 0 0, etc., excluding the 1-st column for the assemblies e_{17} , e_{18} , e_{19} , e_{20} , and e_{21} . For example, in running through e_{16} we would obtain

...0 0 1 1 0 1 0 0.

The preceding arguments show that if upon running through a set from T_{I_0}

the piece $0^* 0$ goes into $1^* 1$, then the 4-th contact of the $(i + 1)$ -th block is short circuited,

the piece $0^* 0$ goes into $1^* 0$, then the 12-th contact of the $(i + 1)$ -th block is short circuited,

the piece $1^* 1$ goes into $0^* 1$, then the 10-th contact of the $(i + 1)$ -th block is open circuited.

An exception is the assembly e_{20} , for when we

run through it, if in the first two columns we have 1 0 instead of 0 0, we have a short circuit in the 4-th contact of the 3-rd block.

Finally, if information I_5 appears, we have $3 \vee 3$. As seen from the table of fault functions and the diagram of the i -th block, to determine the number of the faulty block ($3_i \vee 11_i$) and to detect a short circuit in the 3-rd contact of the i -th block ($i \geq 2$), one must take the assemblies

$$\left(\begin{array}{c} \dots 1^* 1 \dots \\ \dots 0 \ 1 \dots \end{array} \right) \text{ and } \left(\begin{array}{c} \dots 0 \ 1^* \dots \\ \dots 1 \ 1 \dots \end{array} \right).$$

However, unless certain precautions are taken, then in the case of the first assembly the result of shorting of the 3-rd or 11-th contacts of the s -th block ($s \geq i - 2$) may influence the i -th column.

Therefore, the first assembly must have the following form when written in greater detail: $\left(\begin{array}{c} \dots 0 \ 1^* \ 1 \ \dots \\ \dots 0 \ 0 \ 1 \ \dots \end{array} \right)$.

The value 0 in the $(i + 1)$ -th column has as its purpose to block the propagation of the wave arising in the i -th block. It must be indicated here that running through this assembly may lead to a value $\dots 1 \ 1^* 1 \ \dots$ instead of $\dots 1 \ 0^* 1 \ \dots$ not only because of a fault in the i -th block, but also because of a short of the 11-th contact of the $(i + 1)$ -th block. Upon running through the second assembly we can obtain

... 1 0* ... instead of ... 0 0* ... not only because of a closing of the 3-rd contact of the i -th block, but also because of the influence of the backward wave, produced, for example, upon closing of the 3-rd or 11-th contact in the $(i + 2)$ -th block, if the assembly has the form $(\dots 1 0 T^* \dots)$. To prevent the action of the backward wave on the $(i + 1)$ -th block we refine in this assembly the $(i + 2)$ -th column in the following manner: $(\dots 1 0 T^* \dots)$. We can now give the construction of the test T_{15} . We put

$$T_L = (e_{22}, e_{23}, e_{24}, e_{25}, e_{26}),$$

where

$$e_{22} = (\dots 0 1 1 0 1 0 1 1 0 1),$$

$$e_{23} = (\dots 1 1 0 1 0 1 1 0 1 0),$$

$$e_{24} = (\dots 1 0 1 0 1 1 0 1 0 1),$$

$$e_{25} = (\dots 0 1 0 1 1 0 1 0 1 1),$$

$$e_{26} = (\dots 1 0 1 1 0 1 0 1 1 1).$$

These assemblies are based on the repetition of the combinations $(\begin{smallmatrix} 0 & 1 & 1 & 0 & 1 \\ 0 & 0 & 1 & 1 & 1 \end{smallmatrix})$. In the first assembly to insure carry in the second column, we used $\begin{smallmatrix} 1 \\ 1 \end{smallmatrix}$ instead of $\begin{smallmatrix} 0 \\ 0 \end{smallmatrix}$ as the first column. When the network is in proper operating condition, upon running through the foregoing assemblies, the result is an alternation,

from left to right, of the combinations 0 0 and 1 0 1, perhaps with the exception of the first three columns.

Thus, upon running through the assembly e_{24} we have, in the case of a properly working network, ... 0 0 1 0 1 0 0 1 0 0. From the foregoing considerations we conclude that if the piece 1 0* 1, and also the piece 1* 0 1 have become 1 1* 1 and 1* 1 1 respectively, we have a short circuit in the 11-th contact of the i -th block, but if the piece 0 0* has become 1 0*, we have a short circuit in the 3-rd contact of the i -th block.

Note. In running through the assembly e_{25} the piece 1 0 0 plays the same role as the piece 1 0 1: if it becomes 1 1 0, it means either a short circuit of the 11-th contact of the 3-rd block, or a short circuit $3_2 \vee 11_2$ in the 2-nd block.

This completes the construction of the conditional test.

The investigation shows also that all the faults, with the exception of those listed in step II, are pairwise distinguishable. We thus arrive at the following result.

Theorem. To detect a single fault in a one-step binary summator network (see beginning of the section) one can construct a conditional test of length ≤ 13 .

Attention should be called here to the fact that the length of the conditional test is independent of n . The fact that with increasing n , and therefore with increasing number of fault functions, the test does not become longer is due to the increase in the number of network outputs, and consequently, with the increased amount of information obtained at the outputs upon running through the assemblies.

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